Solution-Based Self-Aligned Hybrid Organic/Metal-Oxide Complementary Logic with Megahertz Operation

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Abstract

We have developed a novel solution-based integration scheme featuring organic and metal-oxide semiconductors with a polymeric gate dielectric. The integration relies on a facile subtractive patterning technique for the semiconductors, which, through the selection of an appropriate etch stopper, leads to ideal transistor performance. We utilized this novel integration scheme to fabricate self-aligned transistors and logic circuits with a high mobility p-type conjugated polymer and an n-type amorphous oxide semiconductor, along with a composite polymeric gate dielectric, all solution-deposited by spin coating. The resulting complementary logic gates are capable of rail-to-rail transitions, low-voltage operation down to a 3.5V power supply, and ample noise margins. Thanks to the self-aligned-gate approach and the state-of-the-art balanced mobilities of the selected semiconductors, our logic gates achieve megahertz operation, thus demonstrating the strength of our hybrid integration scheme.

Keywords: Organic thin-film transistors, Metal-oxide thin-film transistors, Self-aligned-gate transistors, Hybrid complementary logic, Solution-processed electronics

1. Introduction

The inherent ambipolarity of organic semiconductors has always sustained the promise of all-organic complementary logic circuit integration [1, 2]. Bringing together a p- and an n-type organic semiconductor pair on the same substrate would indeed help realize the benefits of silicon-like logic circuits in terms of low power dissipation, robust operation, and ease of design [3]. The promise is yet to be fulfilled in a practical manner, however, as the steady progress towards high-mobility p-type organic semiconductors with excellent air stability is not yet matched fully by the n-type counterpart [4, 5]. As a consequence, over the years most investigators resorted to the less desirable unipolar circuit options utilizing one single p-type semiconductor [6, 7, 8, 9]. Top-performance

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implementations of this kind allowed logic-stage propagation delays in the region of the microsecond [7, 8]. All-organic complementary circuits have also been demonstrated by a number of groups, inherently giving much larger noise margins and reduced power dissipation [10, 11, 12]. The inferior mobilities and stability of the n-type organic semiconductors, however, inevitably led to lower speed performance and reliability with respect to the unipolar p-type-only case.

The concurrent emergence of amorphous metal-oxide semiconductors, featuring a far superior n-type performance and stability, led investigators towards hybrid complementary circuit integration, comprising a metal-oxide in combination with a p-type organic semiconductor [13, 14, 15, 16]. The benefits of the complementary approach, together with the choice of top-performance materials from these two classes of semiconductors, generally afforded a higher operational speed and reliability than the all-organic complementary counterpart. All these implementations, however, were based on a bottom-gate geometry with an inorganic gate dielectric not processed from solution, and had at most only one of the semiconductors deposited from solution.

In this study we address the challenge of realizing high-speed and top-performance logic within an approach that allows solution processing of both n-type oxide and p-type organic semiconductors and of a compatible low-temperature gate dielectric. Specifically, we present a process flow in which the complementary pair of top-performance solution-processed semiconductors is integrated on the same chip along with a solution-deposited polymeric gate dielectric.

2. Experimental

We achieved complementary integration through a process flow featuring a top-gate, staggered, and self-aligned architecture. The process flow was devised to allow the solution-based deposition of a p-type organic semiconductor (OS) and an n-type amorphous-metal-oxide semiconductor (AMOxS), both processed by spin coating, patterned subtractively, and capped off with a shared polymeric gate dielectric.

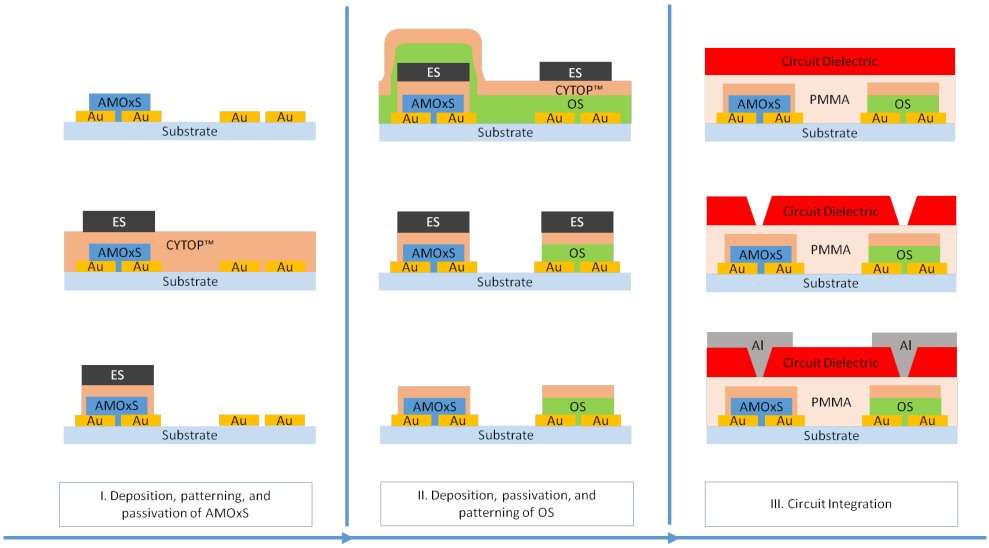
A general illustration of our process flow is shown in Fig. 1. The starting substrate consists of a glass slide on which thermally-evaporated gold source and drain electrodes are defined by photolithography (all patterned with a channel length of $L = 10\mu m$ and a channel width of $W = 1000\mu m$, unless stated otherwise). The amorphous metal-oxide is deposited and patterned first, given its higher processing temperature and superior resistance to solvents, followed by the deposition and patterning of the organic semiconductor. Subsequently, a shared gate dielectric is blanket coated on the sample, and the further processing steps required to achieve the self-aligned gate electrodes is performed as described in [17] (with the aluminum gate electrodes being thermally evaporated through a shadow mask). Finally, circuit connectivity is realized on top of a circuit dielectric (photolithographically patterned S1813™, Shipley Microposit) by opening via holes through it by a combination of photolithography and oxygen-plasma ashing, and by depositing metal interconnects either by thermal

evaporation, or from a commercial silver-based ink (TEC-IJ-050, InkTec Co., Ltd.) with a home-built single-nozzle printer.

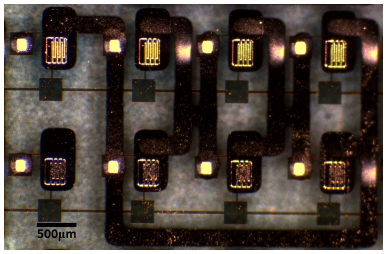
Both semiconductors are blanket deposited by spin coating, and thus subtractive patterning is necessary to confine each of them to the active areas of their respective TFTs (thin-film transistors). The etching of the amorphous metal-oxide is achieved with diluted hydrochloric acid (by conventional lithography), whereas oxygen-plasma is used for the organic semiconductor. While etching the semiconductors, a suitable etch stopper (ES) is required to protect the active regions of the would-be TFTs. We tested two different etch stoppers, one consisting of a photopatterned micron-thick S1813™ film, and another made of a 35nm-thick thermally-evaporated aluminum film (patterned through a shadow mask). To avoid damaging the semiconductors during the etch stopper deposition, a 100nm-thick CYTOP™ (Asahi Glass Co., Ltd.) layer was employed, subsequently patterned by oxygen plasma. At the very end of the semiconductor patterning process, the protective S1813™/aluminum capping off the CYTOP™ islands was stripped by immersion in a suitable solvent (acetonitrile and Shipley's MF-319, respectively), so that the sample could undergo the further steps required for circuit integration.

We implemented this process flow with a particular combination of semiconductors. The organic one we selected is IDT-BT, a top performance p-type polymer which was reported to give hole mobility up to about $2cm^2V^{-1}s^{-1}$ without requiring any high-temperature treatment [18]. The metal-oxide semiconductor used in combination with IDT-BT is a solution-processed alkoxide-based IZO, produced in thin-film form according to the 'sol–gel on chip' detailed elsewhere [19, 20]. Banger et al. characterized the properties of this metal-oxide in bottom-gate inorganic transistors, demonstrating a semiconducting behavior strongly dependent on process temperature, with mobility values in the region of $2 - 4cm^2V^{-1}s^{-1}$ at the lowest reported process temperatures ($200 - 225^oC$) [19]. In order to have balanced semiconductor mobilities for optimum circuit speed, we utilized a process temperature of 250^oC for the IZO, so to match the mobility of IDT-BT in the top-gate configuration.

We performed a preliminary test of our novel integration scheme by realizing transistor arrays with the two kinds of etch stoppers described above. From the structural point of view, we found that both were adequate in producing the desired device stacks. As for the electrical behavior of the resulting TFTs, however, we observed unsatisfactory performance with the S1813™ etch stopper. Typical transistor transfer characteristics for this particular case are shown in Fig. 2a-b. The organic TFTs perform as expected, whereas the metal-oxide ones give currents and mobilities orders of magnitude below their typical performance, and exhibit large hysteresis. In the case of the aluminum etch stopper, instead, structural integrity came along with top-performance transistor behavior. Figure 2c-d shows the resulting transfer curves of representative n- and p-type devices. Both semiconductors give the expected mobilities, and the fact that the transfer curves are approximately mirror-images of each other suggests optimal operation for complementary logic. We thus believe that the perfor-



(a)



(b)

Figure 1: Schematic process flow (a) and top-view of one of our circuit samples (b). In our process flow, the AMOxS is patterned first (via conventional wet etching), and passivated with CYTOP™/ES before undergoing oxygen plasma. A similar procedure is utilized for the passivation and patterning of the OS. Finally, circuit connectivity is realized by means of metal tracks deposited on the circuit dielectric. The specific circuit shown in (b) is a three-stage ring oscillator, whose performance is detailed in Sec. 3.

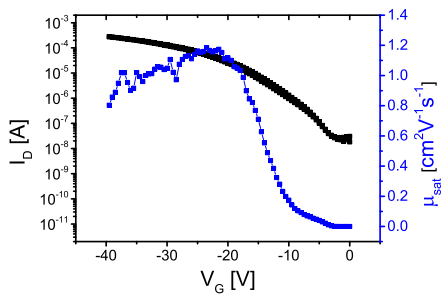
mance degradation of the metal-oxide semiconductor observed with the S1813™ etch stopper results from its insufficient barrier properties with respects to the energetic oxygen-plasma species the sample is exposed to during the patterning steps.

With regards to the aluminum etch stopper, it is noteworthy that the ultra-thin dielectric and organic semiconductor films allow very short oxygen-plasma etching cycles ($7min$ for a $300W$ RF power). Moreover, the aluminum evaporation can be carried out in medium vacuum, as the sole purpose of the resulting films is to act as a barrier against oxygen plasma (e.g., in our system equipped with a $600L/s$ diffusion pump each evaporation cycle takes only $10min$). Therefore, the process utilizing the aluminum etch stopper allows complementary integration with minimal time overhead, and it is thus competitive with the sought-after printing-based integration schemes. Finally, we note that our integration process with the aluminum etch stopper is potentially not limited to CYTOP™ as part or the entirety of the transistor gate dielectric, given that our samples are not exposed to any organic etchant throughout the process. In point of fact, provided their etchability by oxygen plasma, any polymeric dielectric would be suitable, thanks to their well-established compatibility with organic semiconductors, and in the light of their wide applicability to amorphous metal-oxide semiconductors [21]. Our process thus allows a great freedom in the selection of the gate dielectric, and, in particular, paves the way for the adoption of attractive high-κ alternatives for low-voltage operation. For the specific implementation discussed in the following, we employed a bilayer gate dielectric comprising a $100nm$-thick CYTOP™ film topped with a $180nm$-thick PMMA one.

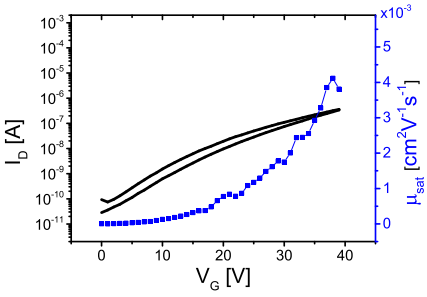
The current-voltage characterization of TFTs and logic gates was performed at room temperature in a nitrogen-atmosphere glovebox (O_2 below $2ppm$ at all times) utilizing an HP4155C SPA (Agilent Technologies). The reported transistor mobility was calculated from the saturation transfer characteristics as $2\left(C_I W/L\right)^{-1}\left(d\sqrt{I_D}/dV_G\right)^2$, where C_I is the transistor gate capacitance per unit area. The time-domain characterization of the ring-oscillator circuits discussed below was carried out with a Tektronix oscilloscope (TDS2014B).

3. Results and Discussions

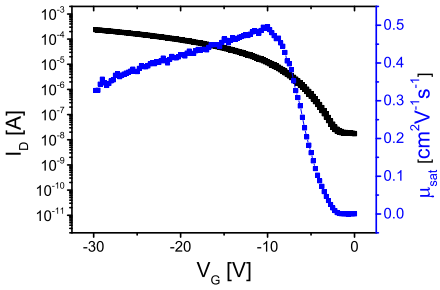
Representative voltage-transfer characteristics (VTCs) of a complementary inverter realized with our solution-based process are shown in Fig. 3a. These VTCs were measured for a range of power supply voltages going from $5V$ to $50V$. Rail-to-rail operation is apparent, even for power supply voltages below $10V$. Although low voltage operation was not among the design goals we pursued (i.e., the dielectric stack we employed consists of low-κ polymers and has a cumulative thickness of $280nm$), the measured VTCs reflect the strength of the complementary approach: as long as the n-type TFT has a much greater current capability than the p-type one, then for a logic high at the input the output



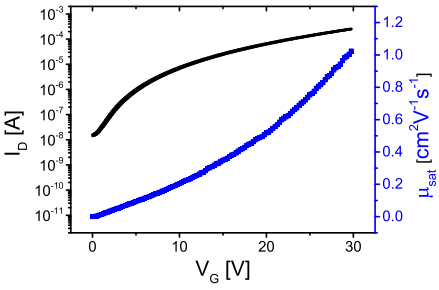
(a) IDT-BT.



(b) IZO (250^oC).



(c) IDT-BT.



(d) IZO (250^oC).

Figure 2: Transfer characteristics and charge-carrier mobilities of the IDT-BT and IZO TFTs produced according to our process flow. (a) and (b) were obtained from a sample patterned with the S1813™ etch stopper, and were measured at $|V_{DS}| = 40V$. (c) and (d) were obtained from a sample patterned with the aluminum etch stopper, and were measured at $|V_{DS}| = 30V$. The minor differences in p-type performance arise simply from batch-to-batch variations.

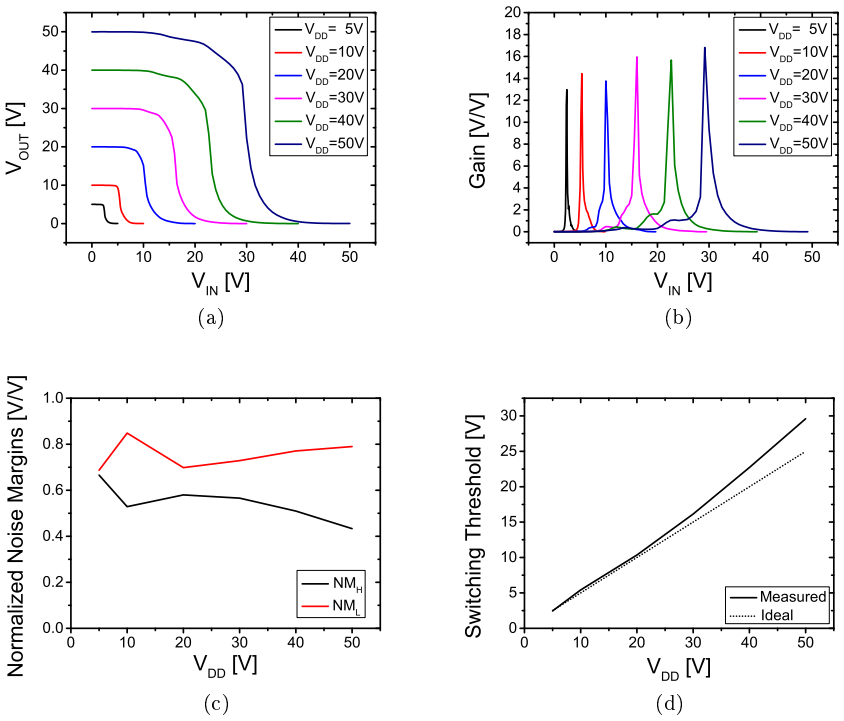
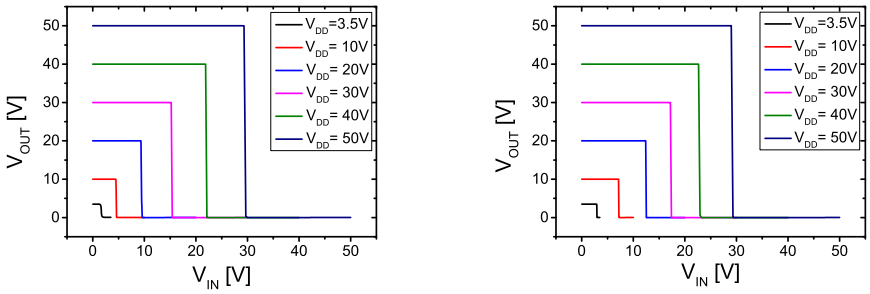


Figure 3: Representative VTCs (a), gain functions (b), normalized noise margins (c), and switching thresholds (d) of our complementary inverters at different power supply voltages.

terminal will be driven to the logic low, even if the transistors are operating in the subthreshold region (and a symmetric argument applies to the opposite set of logic values). The gain functions of our inverters are also shown in Fig. 3b, indicating that a gain above $14V/V$ is consistently observed for power supply voltages greater than $10V$. A peak gain of $16V/V$ is achieved for sufficiently high V_{DD}.

To quantify the robustness of our logic with respect to its ability to reject electrical noise, we extracted the noise margins of our inverters. In particular, we calculated the noise margin for high input, NM_H, and the noise margin for low input, NM_L, which are defined as $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$.[22] Here, V_{IL} and V_{IH} are the input voltages at which $dV_{OUT}/dV_{IN} = -1$ ($V_{IL} < V_{IH}$), V_{OH} is the output high level, namely the output voltage for $V_{IN} = V_{IL}$, and V_{OL} is the output low level, namely the output voltage for $V_{IN} = V_{IH}$. The noise margins of our inverter gates, normalized with respect to the ideal value of $V_{DD}/2$, are shown as a function of power supply voltage in Fig. 3c. Their values are nearly constant and above 50% for most of the



(a) (b)

Figure 4: VTCs of three-stage (a) and five-stage (b) inverter chains.

tested power supply voltage range, with the noise margin for high input being always higher than the one for low input and the gap becoming slightly larger at higher V_{DD}. Such robust noise margins partly arise from the switching threshold staying quite close to the ideal value of $V_{DD}/2$ for all the tested power supply voltages, as shown in Fig. 3d. Furthermore, this confirms that the two equally-sized TFTs in our inverters have symmetric current capabilities thanks to their similar mobilities.

The large noise margins suggest that an inverter of the type presented above should be able to drive a replica of itself. Indeed, we tested this by fabricating inverter chains comprising up to five inverters of the same size. The VTCs of three-stage and five-stage inverter chains are shown in Fig. 4. These plots demonstrate that our hybrid complementary technology has switching capability down to a V_{DD} of $3.5V$, and confirm its robust noise margins. These VTCs exhibit sharp rail-to-rail transitions, with switching thresholds all nearly halfway the power supply voltage.

In order to assess the applicability of our hybrid process to the realization of fast complementary logic, we fabricated ring-oscillator circuits, which give a measure of the propagation delay of an inverter, namely the most basic indicator of the switching speed of a technology. In our ring oscillators, which counted three stages, all equally-sized TFTs had an aspect ratio of $1000\mu m/5\mu m$. The top view of a ring oscillator of this kind is shown in Fig. 1b. The ring oscillators were characterized for a range of power-supply voltages going from $10V$ to $70V$. In order to probe the oscillation frequency without interfering substantially with the ring oscillator operation, we employed an additional p-type TFT whose gate electrode was connected to a node of the ring oscillator. The introduced asymmetry in the loading of the inverters in the ring amounts only to the gate capacitance of an extra TFT, orders of magnitude lower than what would be contributed if a passive probe were connected to the same node to perform

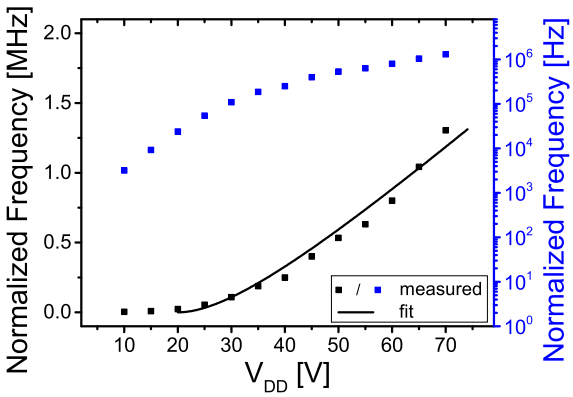


Figure 5: Normalized oscillation frequency of one of our three-stage ring oscillators as a function of the power supply voltage. The black squares represent the measured data in linear scale, and their fit to Eq. 1 is given by the solid black curve. The blue squares, which represent the measured frequency in semilogarithmic scale, are meant to highlight the appreciable oscillation even at low power supply voltages.

the measurement. The drain current of this additional TFT was then fed to an oscilloscope, which allowed us to monitor the oscillation period of the ring. Figure 5 shows a representative plot of the normalized oscillation frequency versus power supply voltage of the inverters in the ring, derived from the measured oscillation through the equation $f_N = 2n/\tau_{osc}$, where n is the number of stages of the ring (i.e., $n = 3$ in our case) and τ_{osc} is the oscillation period. The normalized oscillation frequency f_N is the reciprocal of the propagation delay τ_p of the signal through a single inverter gate in the ring, and is an intensive (i.e., independent from the number of stages) measure of the speed of a technology. The plot in Fig. 5 shows that the normalized oscillation frequency reaches values in excess of $1MHz$ for $V_{DD} > 60V$. We thus observe a performance that is comparable to the work of Bode et al. using UHV-evaporated organic semiconductors [10], and at least an order of magnitude faster than most all-organic solution-processed complementary implementations at equivalent channel length [11, 12]. This speed performance is also well aligned with the most performing hybrid implementation reported thus far, produced by Mourey et al. with ALD-deposited dielectric and AMOxS [15]. In fact, not only our circuits achieve state-of-the-art performance, but also they constitute, to our knowledge, the first realization of hybrid complementary logic utilizing semiconductors and gate dielectric all processed from solution.

An approximate model for an inverter's transient response treats its transistors as constant current sources[23]. Within this picture, for the potential at an inverter's output node to change by $V_{DD}/2$, it would take a time

$$\tau_p^I = \frac{C_L^\dagger V_{DD}}{\mu C_I \frac{W}{L}(V_{DD} - V_T)^2}, \tag{1}$$

where we have assumed that the constant transistor current is equal to its saturation value at $|V_{GS}| = V_{DD}$. Here $C_L^\dagger$ lumps the capacitive load of the inverter, and C_I is the gate capacitance of its component transistors. By fitting the measured switching frequency to Eq. 1, we obtain the solid black curve in Fig. 5, and an estimate of the capacitive load of the single inverter amounting to $C_L^\dagger = 50pF$. Given that in a ring oscillator each inverter is loaded with a replica of itself, and that the calculated input capacitance of an inverter in the ring is $16pF$ ($2A_G C_I$, A_G being the area over which the gate electrode is coupled to the semiconductor), we find that the capacitive load inferred from the fitting procedure is indeed reasonable, especially because the fitting algorithm used here is bound to give $C_L^\dagger > C_L$, C_L being the actual capacitive load of an inverter in the ring. From this we gather that the self-loading in our circuits is minimal (i.e., the capacitance of the transistors in an inverter gives a negligible contribution to the inverter's capacitive load), as we would expect from a self-aligned-gate process. Moreover, we are confirmed that the area of the self-aligned-gate windows is to be kept as small as possible to obtain a high switching speed.

Additionally, the semilogarithmic-scale trace in Fig. 5 shows that reasonably fast transitions ($3.2kHz$ at $V_{DD} = 10V$) occur even for power supply voltages at and below the V_T of the component TFTs (cf. Fig. 2c-d). This comes as no surprise, given the nearly-ideal inverter VTCs we measured for power supply voltages at and below $10V$. At such low voltages, Fig. 5 shows that the normalized switching frequency deviates from Eq. 1. This is in strong analogy with the semilogarithmic-scale plot of a transistor's transfer characteristics: the power-law dependence of the current on the gate-to-source voltage observed above threshold no longer holds in the vicinity of V_T, and an exponential branch is observed further down the gate-voltage axis. Returning to the $f_N - V_{DD}$ trace in semilogarithmic scale, the departure from the power-law dependence of f_N on V_{DD} provides further confirmation of the subthreshold operation of our technology observed in the VTCs in Fig. 3a and Fig. 4. To the best of our knowledge, this is the first report of such behavior in organic/metal-oxide circuits, the great significance of which lies in its potential for ultra-low-power applications.

The excellent static and dynamic performance of our hybrid circuits comes with the added benefit of negligible power dissipation, as allowed by their complementary nature. In fact, our hybrid logic circuits draw no power for constant logic inputs (i.e., static power), and their consumption arises solely during logic transitions (i.e., dynamic power). Referring to the prototypical case of an inverter gate, the dissipation of static power is determined by the current I_{stat} flowing between the supply and ground rails in steady state:

$$P_{stat} = I_{stat} V_{DD} \tag{2}$$

As n- and p- type transistors in one of our inverters are alternatively in

the cut-off region, I_{stat} is limited to the minuscule amount of current flowing through their channel for a zero gate-to-source voltage. Specifically, I_{stat} is equal to the off current through the p-/n- type transistor at $|V_{DS}| = V_{DD}$ for a high/low logic level at the inverter's input terminal. For inverter transistors sized as above and biased at $V_{DD} = 30V$, we have $I_{stat} = 17.3nA$ for $V_{IN} = V_{DD}$ and $I_{stat} = 14.3nA$ for $V_{IN} = 0V$ (cf. transfer characteristics in Fig. 2c and Fig. 2d), resulting in an average static power dissipation of about $500nW$, as given by Eq. 2. On the other hand, dynamic power, dissipated during logic transitions, has a twofold origin: a) the charging and discharging of parasitic capacitances during logic transitions; b) the direct current path between supply and ground rails during the transition time of the input signal. Lumping the parasitics into a capacitive load C_L, the average power consumed in its charging and discharging can be written as

$$P_{par} = C_L V_{DD}^2 f_{clk} \tag{3}$$

where f_{clk} denotes the frequency at which the gate is switched on and off [24]. Moreover, assuming that the inverter input signal has a constant slope and a finite $0-100\%$ transition time t_s, it can be shown that the direct current path during the input signal transients results in the following contribution to the dynamic power dissipation:

$$P_{dc} \approx \frac{V_{DD} - |V_{T,p}| - V_{T,n}}{V_{DD}} t_s V_{DD} I_{peak} f_{clk} \tag{4}$$

where I_{peak} is the peak current flowing through the n- and p- TFTs at the switching threshold, and $V_{T,n}$ and$V_{T,p}$ are their threshold voltages [25]. Both contributions to the dynamic power dissipation are proportional to the circuit clock frequency, given that a higher rate of logic transitions determines a higher number of dissipative events. Considering that the maximum clock frequency of a digital logic circuit is typically $50-100$ times slower than the frequency predicted from ring oscillator measurements[26], we are in the position to estimate the maximum dynamic power dissipated by one of our inverters. Referring to the case of $V_{DD} = 30V$, approximating C_L in Eq. 3 as the input capacitance of an inverter loaded by a replica of itself ($\approx 16pF$), taking I_{peak} as the saturation current of our transistors at the switching threshold ($\approx 30\mu A$), and assuming a transition time for the input signal equal to twice the propagation delay derived from our ring oscillators, we obtain $P_{par}^{max} \approx 30\mu W$ and $P_{dc}^{max} \approx 20\mu W$. We thus observe that, as expected, the power dissipation of our complementary logic is dominated by the dynamic component, which can be more than an order of magnitude higher.

Were we to pursue unipolar integration (e.g., with enhancement-mode saturated load) using one of the semiconductors above, we would incur in much higher power dissipation. Taking into consideration the case of a unipolar inverter gate, a direct current path would exist between supply and ground rails

for one of the logic input levels (i.e., logic high for an n-type implementation), due to both driver and load transistors being on. For the sake of illustration, let us take a load transistor sized with the same dimensions as the ones appearing in our complementary logic gates (i.e., minimum-size transistors). To compute the static power dissipated by such a unipolar inverter, we can still resort to Eq. 2. In the present case, however, I_{stat} is no longer a minute off current, but instead approximately equal to the saturation current at $V_{GS} = V_{DD}$. Referring again to a power supply voltage of $30V$, $I_{stat} \approx 250\mu A$ by inspection of the transfer characteristics in Fig. 2c and Fig. 2d. We would thus have a static power dissipation of about $P_{stat} \approx 7.5mW$. As the dynamic dissipation in unipolar logic gates is around the same level as that of complementary ones for equal operating speed[24], the static component is indeed the dominant source of power consumption in the unipolar logic gates under consideration. In summary, the total power dissipation of the complementary gates realized in our work is at least two orders of magnitude lower than that of the unipolar counterpart. This confirms further the strength of the complementary approach we have pursued: not only does it achieve large noise margins and excellent dynamic performance, but also allows minimal power consumption.

4. Conclusions

We demonstrated a novel solution-based process in which an organic semiconductor, a metal-oxide semiconductor, and a polymeric dielectric are processed on the same chip to give top-gate self-aligned transistors with state-of-the-art performance. The resulting circuits constitute, to our knowledge, the first realization of hybrid complementary logic utilizing semiconductors and gate dielectric all processed from solution. As we employed a subtractive patterning procedure, we showed that the engineering of a proper etch stopper was required to achieve the desired transistor performance. The test logic circuits we realized exhibit rail-to-rail transitions with large noise margins at power supply voltages as low as $3.5V$. Ring oscillators were then used to assess the speed of our specific process implementation, from which we observed megahertz logic-gate operation. Furthermore, we conducted an in-depth analysis of the power consumption of our circuits, confirming their little dissipation thanks to their complementary character. Although our present work was conducted on glass substrates, we believe that our hybrid integration approach based on common polymeric gate dielectrics will also be attractive for realizing hybrid complementary circuits on plastic substrates. The mechanical flexibility of a hybrid circuit comprising only small oxide semiconductor islands but a mechanically flexible polymeric gate dielectric is likely to be superior to that of one that relies on large-area inorganic gate dielectrics like SiO_2 or SiN_x.

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