Scanning Kelvin Probe Microscopy Investigation of the Role of Minority Carriers on the Switching Characteristics of Organic Field-Effect Transistors

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Abstract:

We have developed a Scanning Kelvin Probe Microscopy (SKPM) based method to probe the effects of low-mobility minority carriers on the switching characteristics of organic field effect transistors (OFETs). By measuring and modeling the transient potential changes in the OFET channel after an applied gate bias pulse, we can extract the low mobility of the minority carriers and understand how these carriers play a key role in the device operation, in particular, in the screening of the gate potential in the OFF state of the transistor and in the recombination of majority carriers trapped in the channel after an ON state stress.

Introduction

Many organic semiconductors exhibit intrinsic ambipolar charge transport properties. When tested under suitably inert environmental conditions and in device architectures with gate dielectrics that prevent charge trapping at the interface and source-drain contacts that allow efficient charge injection of both carriers from the contacts, positive hole and negative electron charge carriers in organic field-effect transistor (OFET) measurements exhibit comparable mobilities, that differ typically by not more than an order of magnitude.[1-3] Remarkably, it was found that even the widely-used p-type-only P3HT[1] and pentacene[4-6] are in fact well-balanced ambipolar semiconductors, and that the apparently n-type-only N2200[7, 8] has a substantial hole mobility. However, in many practical device applications, when devices are operated in air or in configurations optimized for one type of carrier, only unipolar conduction is observed, for which one carrier exhibits a high mobility, but the mobility of the other carrier is too small to manifest itself as a measurable current in the measured quasi-DC characteristics of the device.[9-13] Although it is in principle possible for such large mobility differences to be caused by an intrinsic difference in the charge transfer integrals for electrons and holes, in most materials it is likely to be an extrinsic effect due to one polarity of charge carrier being strongly trapped in the semiconductor bulk or at the interface or facing a large injection barrier at the source-drain contacts.

In this work we will refer to the high mobility carriers as "majority" carriers and to the low mobility ones as "minority" carriers although this definition differs from that used in inorganic semiconductors where the notion of majority and minority carriers is defined by the type of doping, whereas organic semiconductors are typically not intentionally doped. The effect of minority carriers, in particular on the hysteresis in the electrical characteristics of OFETs, has been investigated previously for p-type pentacene OFETs.[14-16] However, a direct characterization method of the transport of low-mobility minority carriers is missing and as a result the role of minority carriers in several key aspects of the device physics, such as bias stress and

recovery effects, is poorly understood.

The aim of this work is to investigate how the low-mobility carriers manifest themselves in the switching characteristics of devices that only exhibit unipolar operation. Current-voltage OFET characterization limits the accessible mobility range to values above $\sim 10^{-6}$ cm^2/Vs (estimated based on typical OFF-state, leakage currents). At present no method exists that is able to reliably measure the mobility of minority carriers, if their mobility is lower than $\sim 10^{-6}$ cm^2/Vs. In this work we demonstrate a methodology based on scanning Kelvin probe microscopy (SKPM) that is able to measure directly minority carrier transport. Specifically, by monitoring the spatial and temporal evolution of the channel potential in a unipolar n-type OFET upon step changes of the gate voltage, the injection and transport of the holes were directly visualized. A quantitative analysis of the channel potential transients allows us to measure the low mobility of the minority holes and study their recombination with the majority electrons during charging/discharging processes. While most of the experimental findings presented in the following relate to a specific n-type molecular semiconductor, we illustrate the generality of our findings by investigating as well other representative polymer and small-molecule, n- and p- type organic semiconductors.

Results and Discussion

The n-type semiconductor used in this work is NDI2OD-DTYM2,[17-19] a material with an electron mobility in excess of 0.3 cm^2/Vs. **Figure 1** shows the molecule structure and the diagram of device structures. A preliminary assessment of charge transport in NDI2OD-DTYM2 transistors was conducted via current-voltage characterization. Representative transfer and output characteristics are shown in **Figure 1(c)** and **(d)**, respectively. These curves evidence the behavior of an n-type unipolar OFETs, namely no hole current is detected for negative gate voltages up to 15V in magnitude. Some trapping of electrons during the ON-state operation is evident in the hysteresis in both the output and transfer characteristics. The mobility of electrons extracted in the saturation regime is about 0.1 cm^2/Vs.

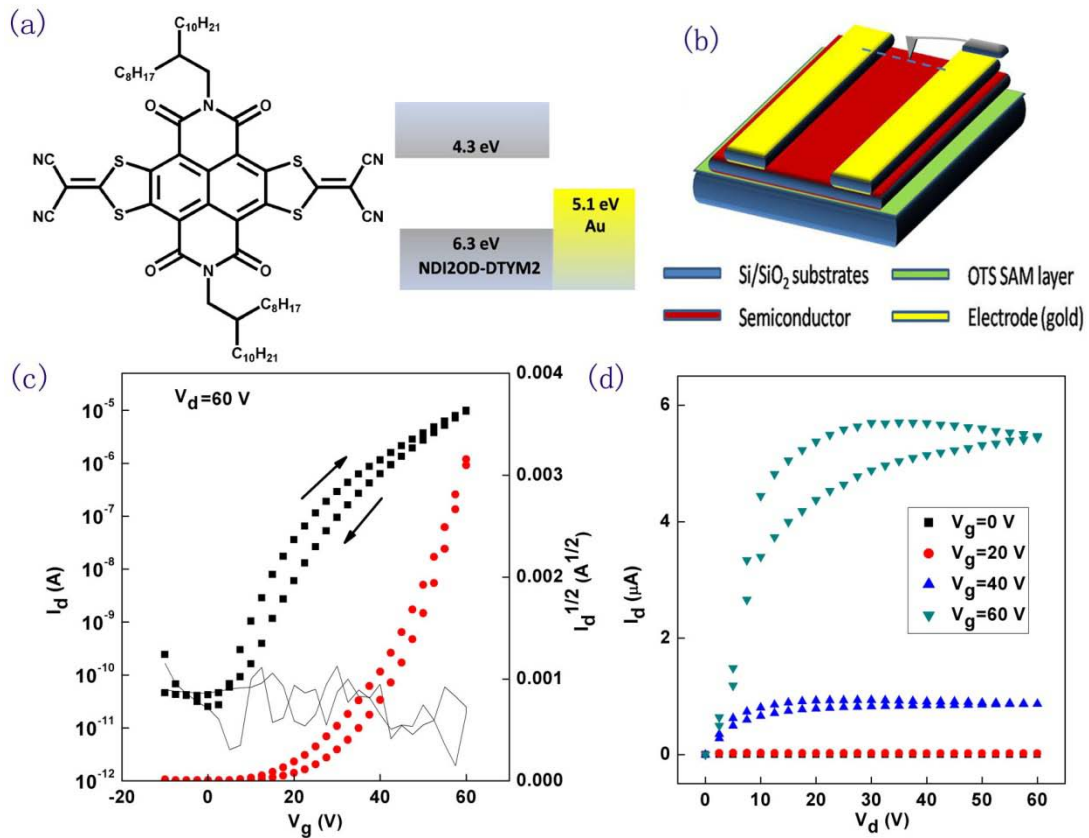**Figure 1** *(**a**)Molecular structure of NDI2OD-DTYM2, and the work function alignment; (**b**)diagrams of the bottom-gate, top-contact devices probed via SKPM;(**c**)a reference device lacking the semiconductor layer;(**c**) and (**d**) representative transfer and output characteristics of an NDI2OD-DTYM2 OFET, respectively. The thin line in (**c**) indicates the gate leakage current.*
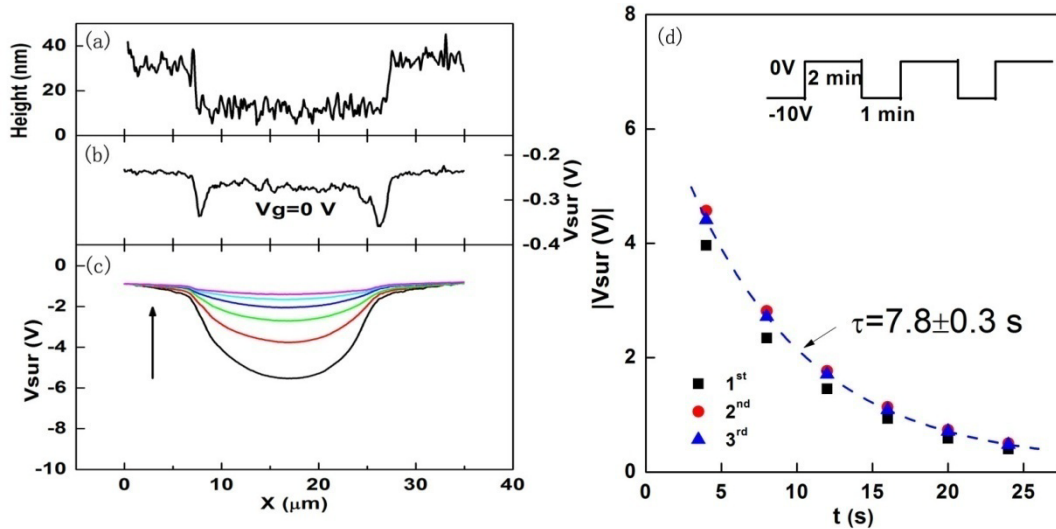
Figure 2 *(a)Line profile of topography and (b)surface potential across the transistor channel with all terminals grounded (V_g = 0 V);(c)Evolution of the channel potential for a negative gate-voltage pulse of –10 V captured every 4 seconds;(d)Evolution of the potential in the middle of the channel((i.e., location of the potential minima in **Figure 2(c)**) for the sequence of negative pulses as indicated in the inset diagram. Here the potential values are the absolute values of the measured potential. The measurements were repeated for three times (1st, 2nd, 3rd) which all gave consistent results.*

An initial set of SKPM measurements involved monitoring the evolution of the channel potential upon application of negative gate-voltage pulses. During these measurements, source and drain electrodes were grounded at all times. The SKPM cantilever scans across the channel with the scanning direction perpendicular to the electrodes, as shown in **Figure 1(b)**. It should be noticed that there is a difference in the probed surface potentials when the cantilever scans parallel to the electrodes due to the coupling effect between the electrodes and cantilever.[20] However, since we used a relatively large channel length (*L*=20 μm) and we are mainly concerned with the potential measured in the middle of the channel, this coupling effect was not taken into account in the following discussions. First the device was measured when zero gate bias applied (V_g = 0 V, baseline bias condition). In this case, the height and potential profiles shown in **Figure 2(a)** and **(b)** were obtained, respectively, with the latter evidencing a small potential difference (≈50 meV) between electrode and

channel regions due to their different work functions.

Upon application of a negative pulse of –10 V, the channel potential initially follows the gate potential and becomes negative, after which a slow decay to 0 V is observed, as shown in **Figure 2(c)**.This measurement was repeated three times to verify the measurement reproducibility (see inset of **Figure 2(d)**) as follows. The gate bias was on (V_g = –10 V) for 1 minute, during which time the potential decay process was measured, and then the bias was off (V_g = 0 V, base line condition) for 2 minutes before it was on again. The transient potential changes are highly reproducible, as evident in **Figure 2(d)** from the close matching of the potential decays in the center of the channel for three consecutive pulses. All traces in **Figure 2(d)** follow an exponential trend of the type $V_s \propto \exp\left(-\dfrac{t}{\tau}\right)$ with a fitted time constant of τ =7.8±0.3 s.

The observed potential decay is indicative of the injection and transport of positive minority holes into the channel, resulting in the gradual screening of the applied gate-voltage pulse. Intuitively, this process can be simply explained as the injection and transport of holes into the semiconductor. With this assumption, the channel potential is a negative value comparable to the applied negative gate bias when there are almost no holes existing in the channel in the initial phase after turning on the negative gate voltage. As more and more holes are injected and transported into the semiconductor, the gate voltage gets screened gradually until the channel potential is 0 V. The analogous process of minority electron injection in p-type OFETs has already been reported previously.[5, 21] It is noted that the first line of the measured potential is about 6 V, which is less than 10 V. This is possibly due to some potential decay having occurred before the first scan and/or due to the limited spatial resolution of the SKPM setup.

An alternative explanation for the observed behavior could be the drift and diffusion of positive ions present at the interface with the SiO_2/Si^{++} substrate.[22] Thus to evaluate whether the positive charge carriers injected into the channel of the NDI2OD-DTYM2 transistors are ionic or electronic in nature, we applied gate voltage

pulses of positive and negative polarity and monitored the potential profile along the channel over time in a reference device.(see supplementary **Figure S1**).However, the Kelvin probe measurements show that there is no potential decay upon applied gate bias in the reference device, which unambiguously demonstrates that the channel potential decay in the NDI2OD-DTYM2 transistors does not arise from ionic transport on the surface of the SiO_2 dielectric or within the SAM layer, but is to be attributed to electronic minority carriers in the organic semiconductor.

Next, we investigated the case when a negative gate bias was switched off in the n-type OFETs. In this case upon transiting from a gate voltage of –10 V back to 0 V baseline bias condition, the channel potential does not undergo a slow decay, and instead immediately reaches 0 V at all points. This implies that either the minority holes could leave the channel quickly, *i.e.* faster than the time resolution of the SKPM, or, more likely, that fast majority electrons can be injected into semiconductor quickly to recombine with the slow holes. It should be mentioned here that the due to the limit of the scanning speed of SKPM, the time resolution is on the order of a few seconds. So any physical process happens in a faster time scale than that would not be captured. Also due to limitation of our instrument with a measurable range of only ±10 V, the channel potential that is larger than 10 V cannot be measured.

After examining the transient response of the channel potential to a negative gate-voltage step in the above section, we now shift our focus to voltage steps of opposite polarity, which we expect to result in electron injection into the channel. In the same fashion as the SKPM experiments introduced above, we monitored the channel potential upon application of a sequence of 1-minute-long positive gate-voltage pulses($V_g = +30$ V) spaced away by 2-minute-long periods at the baseline bias condition($V_g = 0$ V).
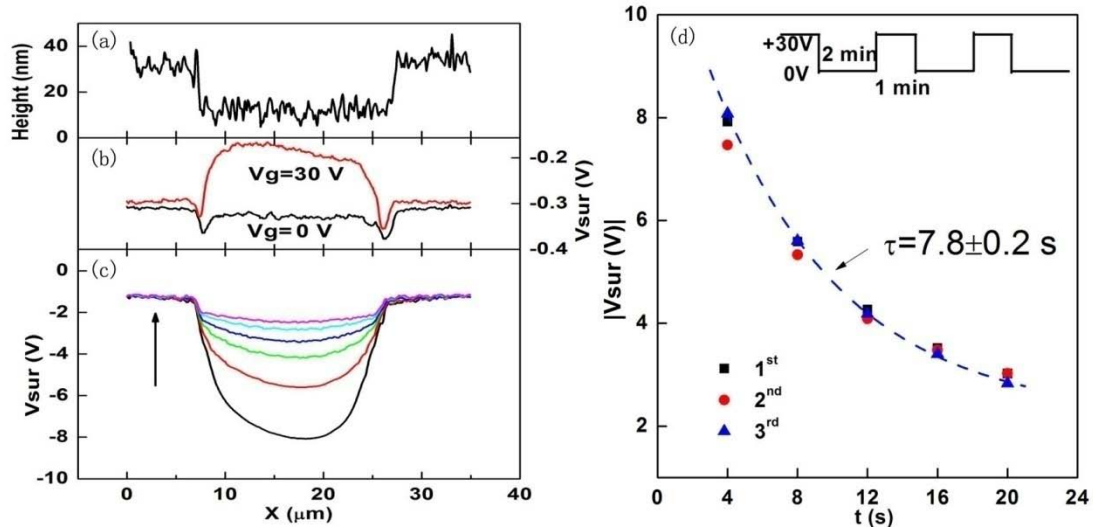
Figure 3(*a*)*Line profile of topography and* (*b*)*potential profiles along the channel region at the baseline bias condition* ($V_g = 0$ V) *and for a positive gate bias of* $V_g = +30$ V; (*c*)*Evolution of the channel potential after switching off a positive gate-voltage pulse of +30 V; It is noticed that there is an asymmetry in the potential profiles, especially when the potential values are large. We think this is an experimental artifact caused by the delay during the scanning process. Specifically, when the tip scan from right to left, there is already some potential decay in the left and so the left and right are asymmetric.* (*d*)*Evolution of the potential in the middle of the channel (i.e., location of the potential minima in* **Figure 3(c)**) *after the switching off* $V_g = +30$ V. *The graph shows the results of three repeated measurements.*

Upon application of a positive pulse, the SKPM probe reveals that the gate bias is screened instantaneously, with the channel potential returning to close to 0V on the first potential scan after switching on the device as shown in **Figure 3(b)**. The only observable variation with respect to the baseline bias condition is an increase of about 0.1 eV to a more positive potential value, reflective of the Fermi level shift in the semiconductor associated with the filling of the density of states by injected electrons.[23] This is in contrast with the slow transient under hole accumulation discussed in above, and is consistent with the n-type character of NDI2OD-DTYM2 FETs, which allows a fast charging of the channel with high mobility majority electrons. Given the magnitude of the electron mobility of NDI2OD-DTYM2 (≈0.1 cm^2/Vs), we expect the electron channel to be formed over a timescale of the order of

microseconds, as can be estimated via the model developed by Burgi *et al.*.[24] Since the time resolution of the SKPM setup used here is on the order of seconds, the electron-channel formation is indeed too fast to be resolved.

When switching the gate voltage from its positive ON-state value to 0 V we detected initially a negative potential of close to –8 V in the middle of the channel followed by a slow decay towards 0 V as shown in **Figure 3(c)**. A plot of the potential transient in the middle of the channel reveals an approximately exponential decay with a characteristic time constant $\tau = 7.8\pm0.2$ s.

Immediately after the switching from $V_g = +30$ V to 0 V a potential of –30 V would have been expected in the channel. This potential should then quickly drop on a time scale faster than the time resolution of our SKPM measurements as mobile electrons leave the channel.[24] The fact that a residual negative potential of close to –8 V remains after a few seconds is likely due to a fraction of the gate induced concentration of electrons becoming trapped during the ON-state operation and remaining in the channel after turning the device off. The presence of such trapped electrons is consistent with the observation of hysteresis in the device characteristics **in Figure 1(d)**. We note that the residual negative potential in the first acquired trace (black trace in **Figure 3(c)**) cannot be explained with the limited time resolution of our SKPM measurements ($t_{res} = 4$ s). Actually, an extrapolation of the transients in **Figure 3(d)** to a time t_{res} earlier than the first measured data point yields a potential value still well below 30 V in magnitude. In fact, the channel potential extrapolated to $t = 0$ s (when the gate bias was switched off) is estimated to be about 20 V, which is consistent with the threshold voltage values obtained from the transfer curves, indicating that measured potential is indeed produced by the trapped electrons.

One might expect the slow potential decay from –8 V to 0 V to reflect the slow release of these electrons from their trap sand their migration out of the channel. This electron detrapping process would involve an independent physical process from the slow minority carrier transport that governs the screening of a negative gate potential (cf. **Figure 2(d)**) and would therefore be expected to occur on a different timescale. What is surprising is that the time scale of the slow potential decay after a positive

gate voltage is switched back to 0 V is in fact very similar to that of the screening of a step in the gate voltage to negative values, *i.e.*, both processes occur on a time scale of $\tau = 7.8$ s. This correlation holds more generally for a wide range of NDI2OD-DTYM2 transistors fabricated under different conditions. The temperature at which the NDI2OD-DTYM2 films were annealed influenced the timescale of the slow potential decay, but remarkably it influenced both processes in the same way such that the slow dynamics of electron-channel discharging and hole-channel charging remain comparable, even though they are not exactly the same any more(See **Figure 4** and more discussions in SI).This gives a strong indication that the two phenomena are in fact related to the same physical process, *i.e.* the injection and transport of slow minority holes into the channel.

On the basis of the arguments above, we propose the following mechanism to rationalize the complex dynamics of electron-channel discharging in NDI2OD-DTYM2 transistors. Our results suggest that this process does in fact not reflect the release process of trapped electrons from their trap state, but the transport of slow minority carriers into the channel and involves the following steps:

1) fast migration of mobile electrons out of the channel;
2) slow hole injection and transport into the channel under the influence of the electric field created by the negative space charge of trapped electrons left behind in the channel;
3) recombination of injected holes with trapped electrons.

The initial migration of mobile electrons is invoked to explain the initial fast dynamics of the discharging transient and is expected to occur within a timescale of tens of microseconds considering the high electron mobility of NDI2OD-DTYM2. The remaining, trapped electrons are in states that are too deep to be released effectively on a timescale of seconds, but will concurrently attract holes into the channel. The transport of these holes thus dictates the slower dynamic of the discharging transient. The two types of carriers will eventually recombine, thus resulting in the observed channel potential decay. We note that the notion of the process of detrapping occurring by a recombination process is fully consistent with

the results of light-assisted trap release in OFETs reported by Burgi *et al.*.[25] In that work, the detrapping mechanism is explained in terms of the recombination of trapped carriers with carriers of opposite polarity created upon photo-excitation.

We summarize our understanding of the physical processes that take place in unipolar OFETs when a positive or negative gate bias is switched on or off. Taking an n-type OFET as an example, when a negative gate bias is switched on, holes are accumulated in the channel, a process involving the injection and transport of holes in the n-type semiconductor. Since the mobility of minority holes is rather low in the n-type semiconductor, the gate bias screening or hole charging process, may take tens of seconds. When the negative gate bias was switched off, the holes cannot discharge from the channel timely and thus electrons will be induced into the channel to recombine with the holes. Similarly, when a positive gate bias is switched on, electrons are induced in the channel and this process finishes almost instantaneously(on the order of μs) because the electron mobility is high. The physical process after the positive gate bias is switched off involves the rapid discharge of un-trapped electrons from the channel, the subsequent, slow injection and transport of minority holes into the channel followed by recombination with trapped electrons. **Figure S2** in supplementary illustrates these four charging and discharging processes in an n-type OFET.

For a more quantitative analysis of the transport properties of minority carriers we developed a model of the injection and transport of holes in the n-type semiconductor. The physics behind this process is quite similar to that reported by Burgi.[24] In that work, mobile hole majority carriers were injected and transported into the channel when a negative gate voltage was applied to P3HT metal-insulator-semiconductor device. A drift-diffusion equation (1) was used to describe the drift and diffusion process.

$$\frac{dp}{dt} = \frac{\partial(\mu_p pE + D_p \frac{\partial p}{\partial x})}{\partial x} \quad (1)$$

In the equations above, p is the hole volume density, q is the elementary charge, μ_p is the hole mobility, E *is* the electric field in the channel, and D_p is the diffusion constant

of holes, which we later assume to follow the Einstein relationship. Here, we simplified the problem to be one-dimensional (1D) and x denotes the direction across the channel. In the FET structure, the charge density and the channel potential V_s are directly related via:

$$p = \frac{C_i}{qt_{acc}}(-V_g + V_{sur}) \quad (V_g < 0, V_{sur} < 0) \, (2)$$

Where C_i is the insulator area capacitance and t_{acc} is the thickness of the accumulation layer. Combing equation (1) and (2), the temporal evolution and distribution of channel potential V_{sur} can be solved readily.

However, to fully simulate the whole injection and transport process of holes, the injection barrier or the contact resistance also has to be considered. A significant hole injection barrier is indeed expected because of the large offset between the Fermi level (5.1 eV) of the gold source and drain electrodes and the HOMO of NDI2OD-DTYM2(6.3 eV). Moreover, the SKPM data shows that the electric filed strength (*i.e.* the first derivative of potential V_{sur} over x) is rather large at the semiconductor-electrode interfaces, suggesting the existence of an injection barrier (as shown in **Figure S4**). To deal with the injection problem without introducing new fitting parameters, that might obscure the extraction of the minority carrier mobility values, we restrict our simulations to the potential data points between the positions where the electric field strength is maximum and we use the values of the measured surface potential at the electric field maxima as boundary conditions for the simulation. In this way, the influence of contact resistance is then included in the boundary conditions and we just need to solve the PDE equation (1) to model the surface potential or charge distribution in the channel, which was carried out in MatLab and involved a single fit parameter, the minority carrier mobility.

Figure 4(d-f) shows the numerical solution of the channel potential V_{sur} when a gate bias $V_g = -10$ V was applied together with the experimental data for films annealed at different temperatures. The simulation results fit the experimental data reasonably well (for a more detailed comparison see SI). For the film annealed at 120°C we extract a minority carrier mobility of $\mu_p = 8 \times 10^{-9}$ cm^2/Vs. The extracted hole

mobility is very low compared to the electron mobility, in fact it is so low that no hole current-voltage characteristics can be measured in the n-type semiconductors. We speculate that this may be due to extrinsic trapping of holes arising from ambient species, as expected for a semiconductor with a rather deep HOMO (about 6.3 eV).[18, 26] So, our SKPM measurements and modeling methods thus provide an elegant and direct way to probe the hole transport in n-type semiconductors, or more generally, the transport of the minority charge carriers in organic semiconductors.
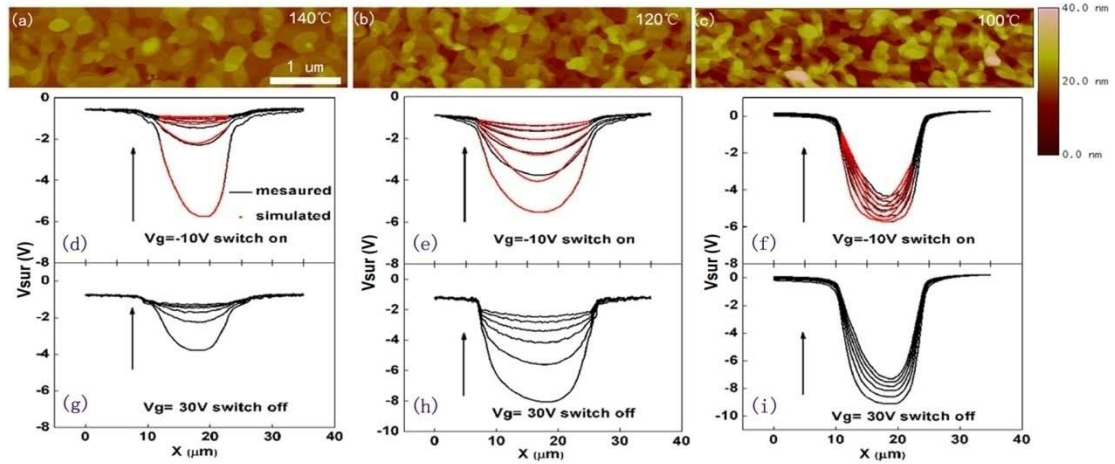

Figure 4(*a-c*)*The morphology of the NDI2OD-DTYM2 films annealed at 140°C, 120°C and 100°C, respectively;(**d-f**)The corresponding measured and simulated transient potential distribution V_{sur} in the channel for devices annealed at different temperatures when $V_g = –10$ V was switched on. The black lines are the experimental data while the red symbols are the simulated data;(**g-i**) The measured transient potential distribution V_{sur} in the channel when $V_g = +30$ V was switched off.*

We can also use the model to simulate the different decay rates of channel potential in devices fabricated for different semiconductor annealing temperatures. As shown in **Figure 4(d-f)**, it is found that simulation results are consistent with the experimental data, and the hole mobility increases in devices annealed at higher temperatures. These results not only confirm the idea that the hole mobility is dependent on the film structure or morphology, namely the films annealed at lower temperature contains higher concentration of extrinsic traps that slow down the hole transport, but also again show the validity of our modeling methods.

The injection and transport of the minority charge carriers is found to be quite general phenomena in organic semiconductors. In our work, we observed the injection of low mobility minority electrons in p-type, unipolar 2,7-dioctyl [1]benzothieno[3,2-b]benzothiophene (C8-BTBT) FET. As is well known, C8-BTBT is a high-mobility p-type molecular semiconductor.[27, 28] Yet there is no report of electron transport in this material. In our SKPM measurement, it was seen that the potential channel slowly decays from a positive value to 0 V when a positive gate bias was applied. Similarly, when a negative gate bias was switched off, the residual potential in the channel also decays slowly from a positive value to 0 V. These phenomena are quite consistent with what we have observed in the n-type semiconductors, implying the injection and transport of minority electrons in this material.

We also measured some polymer semiconductors in similar ways. Interestingly, the slow potential decay features in SKPM were not seen in the polymers when applying or switching off gate bias. For instance, in poly (2,5-bis (3-tetradecylthiophen-2-yl) thieno[3,2-*b*] thiophene) (pBTTT)[29, 30] FET, the channel potential responded quickly with a small increase when a positive gate bias was applied (as shown in **Figure S7**). This shows that there is still injection and transport of electrons in this material to screen the gate bias, but the process occurred so quickly that SKPM cannot capture the potential change process. Similarly, no potential decay process was observed when the negative gate bias was turned off, again indicates the quick injection and transport process of electrons. These results are understandable because generally polymer semiconductors have smaller band gap, and so easier ambipolar transport is expected in these materials compared to small-molecule semiconductors.[31-33] It is estimated from the above simulation results that once the charge carrier mobility is higher than 10^{-7} cm^2/Vs, our current SKPM setup will not be able to characterize the potential decay process any more. Of course, the technique could be extended to higher mobility values by improving the time resolution of the experiment.

Conclusions:

To summarize, we have used SKPM to probe the injection and transport of low-mobility minority carriers in organic semiconductors, an evaluation of which is essential for a comprehensive understanding of the device physics of unipolar OFETs. Low-mobility minority carriers, such as electrons in p-type semiconductors or holes in n-type semiconductors, cannot be probed by conventional current-voltage characterization. Our generally applicable SKPM-based method measures the transient channel potential decay process upon switching of the gate voltage. A simple 1D drift-diffusion model provides an estimate of the minority carrier mobility. An important insight gained from our work is that after a period of ON-state operation the time scale in the OFF-state on which a space charge due to trapped majority carriers is removed from the channel is not governed by the thermal release of majority carriers from their trap states but by the injection and drift-diffusion into the channel of slow, minority holes. This mechanism implies an interesting strategy to improve the recovery kinetics for threshold voltage shifts in OFETs stressed in their ON-state for a prolonged period of times. If the threshold voltage shift is caused primarily due to majority carriers being trapped in the active semiconductor layer, its recovery after turning off the stress can be accelerated by improving the contact injection and charge transport properties of the minority carriers. This strategy might lead to improved lifetime of OFETs in practical applications.[34]

Experimental Section:

Device fabrication: Devices were fabricated in a bottom-gate, top-contact configuration on SiO_2/Si^{++} substrates. To ensure a semiconductor/dielectric interface with low defect density, the SiO_2 surface was modified with octadecyltrichlorosilane (OTS). Semiconductor films were formed by spin-coating the NDI2OD-DTYM2 solution with a concentration of 10 mg/ml in chloroform. The films were subsequently annealed in ambient atmosphere for 10 minutes. Finally, gold source and drain electrodes were evaporated through a shadow mask defining a channel of length

$L = 20$ μm and width $W = 1$ mm. A similar structure was used for the fabrication of the reference devices, which differ from the full transistors only in their absence of a semiconductor layer.

Current-Voltage Characterization: Transistor current-voltage characterization was conducted in a nitrogen-atmosphere glovebox with an HP4155C SPA (Agilent Technologies).

SKPM measurements: Kelvin probe measurements were carried out with a Veeco Dimension 3100 AFM system in ambient atmosphere. This system was selected because of its capability to scan over a length scale up to 80 μm, thus allowing the mapping of the potential distribution across the entire channel of our transistors. The measurements were conducted with a scanning rate of 500 mHz, which corresponds to a time resolution of 4 s for the potential reading at each point of the transistor channel.

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