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Programmable logic circuits for functional integrated smart plastic systems

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ABSTRACT

In this paper, we present a functional integrated plastic system. We have fabricated arrays of organic thin-film transistors (OTFTs) and printed electronic components driving an electrophoretic ink display up to 70 mm by 70 mm on a single flexible transparent plastic foil. Transistor arrays were quickly and reliably configured for different logic functions by an additional process step of inkjet printing conductive silver wires and poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS) resistors between transistors or between logic blocks. Among the circuit functions and features demonstrated on the arrays are a 7-stage ring oscillator, a D-type flip-flop memory element, a 2:4 demultiplexer, a programmable array logic device (PAL), and printed wires and resistors. Touch input sensors were also printed, thus only external batteries were required for a complete electronic subsystem. The PAL featured 8 inputs, 8 outputs, 32 product terms, and had 1260 p-type polymer transistors in a 3-metal process using diode-load logic. To the best of our knowledge, this is the first time that a PAL concept with organic transistors has been demonstrated, and also the first time that organic transistors have been used as the control logic for a flexible display which have both been integrated on to a single plastic substrate. The versatility afforded by the additive inkjet printing process is well suited to organic programmable logic on plastic substrates, in effect, making flexible organic electronics more flexible.
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1. Introduction

When the organic field effect transistor (OFET) was first fabricated in 1987 [1], the Intel 80386 was the established microprocessor of the day with a minimum channel length of 1.5 μm and 275,000 transistors in an area of 104 mm^2 [2]. 25 years later, the 2,600,000,000 transistors of the state-of-the-art 10-core Intel Xeon are accompanied by a minimum channel length of 32 nm in an area of 512 mm^2[2]. Meanwhile, there have also been notable advances in the large scale integration of organic transistors. Recent publications have demonstrated circuit functions such as 8-bit, 64-bit and 128-bit radio frequency identification (RFID) tags [3–5], and 8-bit microprocessors with 3381 transistors at a channel length of 5 μm [6]. These achievements, roughly comparable to the Intel 4004 of 1971 [2], are expanding the current envelope of integrated organic transistor circuit designs while also demonstrating the benefits of organic transistor technology such as flexibility, low temperature fabrication, and solution processing.

In order to alleviate the often prohibitive time and expense of silicon chip design and fabrication, semi-cus-

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tom and programmable logic devices are often used instead of full custom multiple mask set designs. With semi-custom designs, a mask set for a generic array of transistors is used to partially fabricate the device, requiring only a final metal layer mask (or masks) which customises the function. In this way, the costs of the shared masks are spread over all applications and only the cost of the final customising mask is additional. Alternatively, for a programmable device, the entire mask set is made and the chip is fabricated but a customised function is then programmed in the final device. There are several ways to accomplish the programming such as Erasable Programmable Read Only Memory (EPROM), Electrically Erasable Programmable Read Only Memory (EEPROM), Static Random Access Memory (SRAM) or antifuse [7].

In this paper we show an approach to complex functions fabricated with organic electronics which uses a programmable array of organic thin-film transistors (OTFTs) and makes best use of an additive manufacturing step, in this case, inkjet printing. Inkjet printing offers the advantages of a maskless on-demand processing step which allows low-cost, quick and accurate placement of functional wires and components. Inkjet printing has been previously used to create a Print-Programmable Read-Only Memory (P^2ROM) for use as an instruction generator in a hybrid oxide-organic complementary microprocessor system [8]. We demonstrate two architectures of programmable arrays which can be customised by final printing steps. We also highlight the advantages of organic processing by integrating a simple, flexible display on to the same plastic foil substrate as the fabricated transistors and printed electronics, driven only by the array of organic transistors. Four different circuit designs are presented with these two different array architectures. The first programmable array architecture is an uncommitted transistor array whose devices can be connected with a single final level of inkjet printed wires and resistors to form logic functions. Three circuit designs on this first programmable array architecture highlight key building blocks necessary for more complex logic circuits, namely (i) a ring oscillator, (ii) a memory element, and (iii) a pass-code checker. The second programmable array architecture is a full-featured programmable array logic device (PAL) comparable with commercially available silicon simple programmable logic devices (SPLDs) featuring 8 inputs, 32 product terms, and 8 outputs with macrocells consisting of memory and selectable inverters. A single circuit design of a 2:4 demultiplexer driving an electrophoretic ink (E-Ink) display was demonstrated on this second programmable array architecture.

2. Experimental

To demonstrate functional integrated plastic systems (FIPS), 2 different programmable array architectures were designed and fabricated on separate plastic foils. Transistors with a channel length of 5 μm of the same construction as used in Plastic Logic's high yielding and uniform active matrix display manufacturing process [9,10] were designed as either an array of transistors or as logic blocks programmable by inkjet printing. To complete the integration of the foils, an E-Ink display supplied by E Ink Corporation and inkjet printed wires and resistors were added. Our work provides a first example of how an OTFT manufacturing process developed by Plastic Logic for display applications and optimised for high transistor yield and uniformity over large-area flexible substrates can be used for large-scale logic circuit integration.

2.1. Foil 1 programmable array architecture description

The first foil (FIPS1 - Fig. 1) consisted of a transistor array and a 4-shape E-Ink display. The transistor array was an 18 × 3 array of 54 transistors of 3 different widths with which a function could be implemented by inkjet printing a single layer interconnect pattern in conductive silver ink (Inktec TEC-IJ-050). Using our own custom software to interface between the computer aided design (CAD) system and the inkjet printer, we were able to reliably design and print interconnect patterns of up to 344 individually printed wires. Three of the circuits presented in this paper are examples of the speed and versatility of this method using this programmable array architecture; namely, a 7-stage ring oscillator, a flip-flop memory element, and a pass-code checking circuit with finger-touch sensors and different printed resistor values. All digital circuits have been designed using diode-load logic with p-type transistor devices [11].

The E-Ink display (Fig. 1) consisted of 4 geometric shapes; a circle, a triangle (not displayed), a square, and a pentagon. Each shape was able to be independently switched on (black) or off (white) by application of a voltage which was positive (on) or negative (off) with respect to a mid-rail common voltage.

2.2. Foil 2 programmable array architecture description

The second foil (FIPS2 – Fig. 2) greatly increased the sophistication of FIPS1 by incorporating a complete implementation of a PAL with a patterned graphic, directly driven E-Ink display of 100 μm resolution. The PAL was configured as a conventional AND-OR array with a fully programmable AND-array and fixed OR-array. The programming of the PAL was accomplished by accurate printing of conductive wires at a 250 μm pitch in a switch fabric between the functional blocks of the PAL (Fig. 3). In addition to the PAL of the FIPS2 foil, some pre-configured standard circuits were also incorporated. These were a 9-stage ring oscillator with divide-by-2 frequency dividers, and a 2:1 clock selector. (As yet, these additional components have not been incorporated into any circuit designs using the PAL.) There were a total of 1260 transistors on FIPS2.

The patterned graphic E-Ink display had 3 interleaving designs. These can be seen on Fig. 2 as a thin vines pattern, a broader swirls pattern, and the background pattern which includes neither the vines nor the swirls. As with FIPS1, each pattern can be independently switched on (black) or off (white).

2.3. Fabrication

The fabrication of the foils was performed jointly by Plastic Logic and the University of Cambridge. The

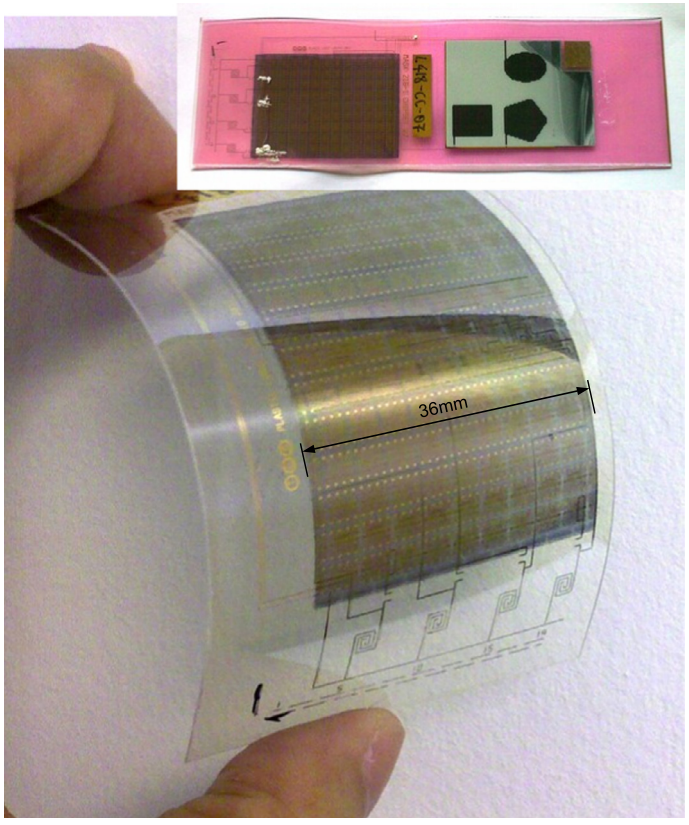


Fig. 1. Photograph of a delaminated FIPS1 sample showing the transistor array with printed silver wires and PEDOT:PSS resistors. Four touch sensor pads are visible at the bottom of the foil. Inset shows a FIPS1 foil still on glass with the 40 mm × 40 mm E-Ink display.

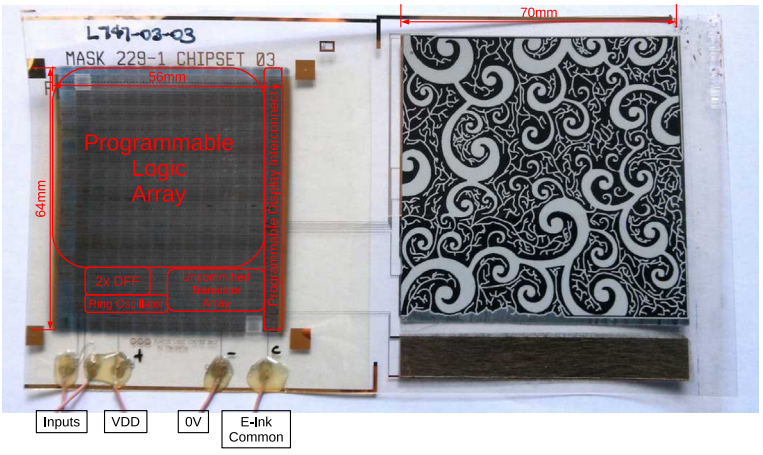


Fig. 2. Photograph of the 2:4 demultiplexer demonstrator implemented on the PAL of a delaminated FIPS2 sample with its 70 mm × 70 mm E-Ink display on the same flexible plastic substrate. In this picture, the vines and swirls patterns are white while the background pattern is black. The input, power and E-Ink connections are shown for the 2:4 demultiplexer demonstrator.

fabrication process, summarised in Fig. 4, began with a planarised sheet of 125 μm (FIPS1) or 50 μm (FIPS2) polyethylene naphthalate (PEN), glued on to a glass carrier. After the source and drain metal electrodes were sputtered on to the PEN substrate and patterned by photolithography, a solution of a p-type organic polymer semiconductor was deposited, followed by gate dielectric deposition. After sputtering and patterning of gate metal, a 2 μm insulating layer was added. Then a final top layer of metal was sputtered and patterned for the 3-metal layer process. Connections from the bottom source-drain metal layer to either the gate-metal layer or the top-metal layer were

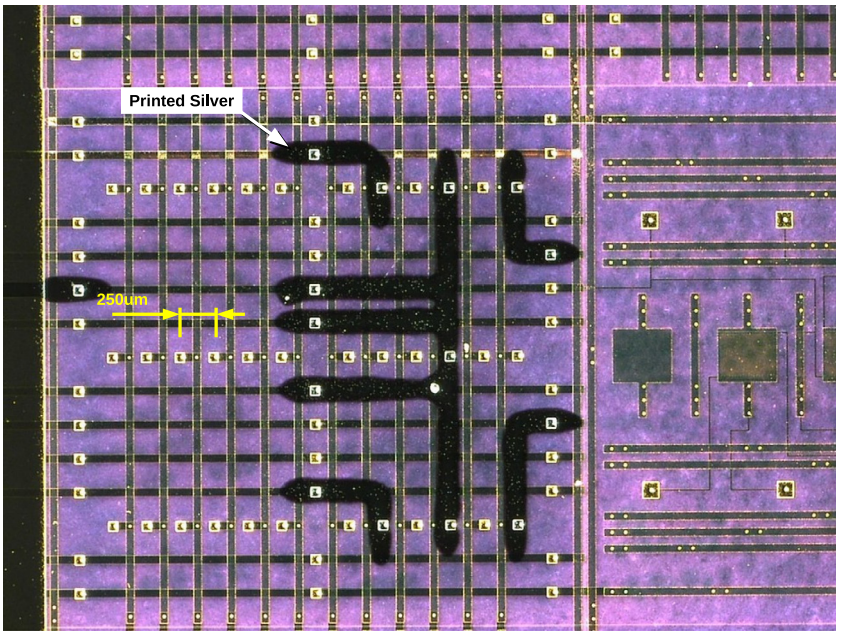


Fig. 3. Micrograph of printed silver wires used in the PAL on the FIPS2 sample.

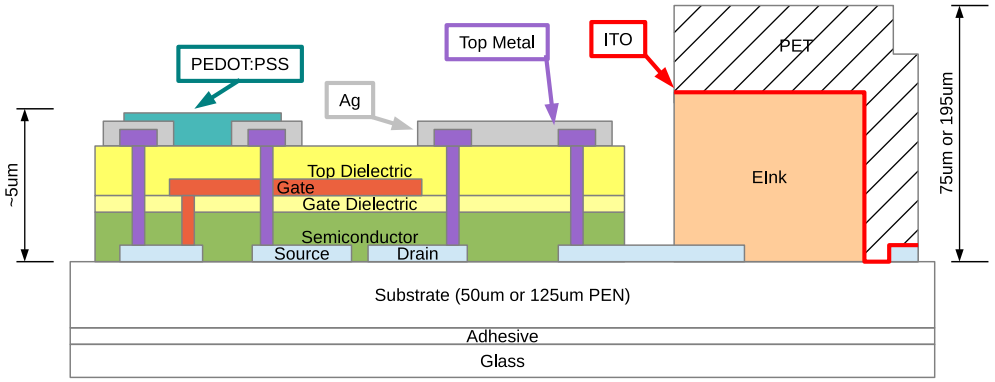


Fig. 4. Process summary (not to scale).

accomplished by laser ablated vias. Adjacent to the transistor array, an area of the PEN substrate had been tape-protected from the processing steps following source-drain metallisation. This area was now cleaned and prepared for E-Ink lamination with the suitably patterned source-drain metal in this area providing signal connections to the E-Ink. The E-Ink display medium on FIPS1 was 40 mm by 40 mm, 195 μm thick, and for FIPS2, 70 mm by 70 mm, 75 μm thick. The final step was the inkjet printing of conductive silver wires and poly(3,4-ethylenedioxythiophene):poly(styrene sulfonate) (PEDOT:PSS) (Clevios PH1000, Heraeus) resistors using a custom printer with a single nozzle piezo-electric print-head and with 30 μm (silver wires) or 40 μm (resistors) nozzles from Microfab [12]. Finally, the PEN foil was delaminated from the glass carrier to leave the flexible transparent circuit and display. A micrograph of printed wires and resistors is shown in Fig. 5. All measurements were performed in air in ambient conditions by an Agilent 4156C Semiconductor Parameter Analyser (SPA) and an Owon PDS5022S portable digital storage oscilloscope.

3. Results and discussion

To investigate different functions, 4 different circuits of increasing complexity were designed and printed on the 2 array architectures.

3.1. Ring oscillator

A 7-stage ring oscillator was designed and printed on the FIPS1 array architecture, the results of which are shown in Fig. 6. Two 7-stage ring oscillators were actually printed on the same foil, comprising a total of 344 individually printed conductive silver wires. Two novel aspects of our ring oscillator were the use of a 2-input NAND gate as the first inversion stage, and the provision of identical

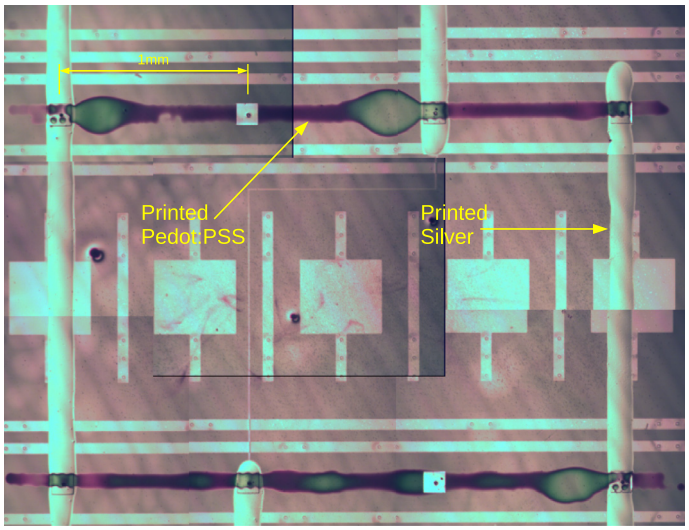
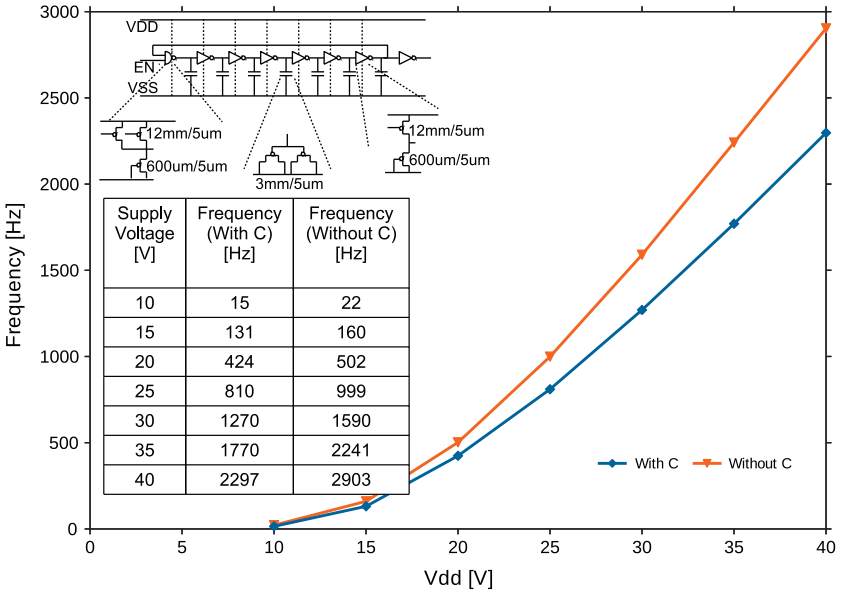


Fig. 5. Composite micrograph of inkjet printed silver wires and PEDOT:PSS resistors.



Supply Voltage [V]	Frequency (With C) [Hz]	Frequency (Without C) [Hz]
10	15	22
15	131	160
20	424	502
25	810	999
30	1270	1590
35	1770	2241
40	2297	2903

Fig. 6. Schematic and measurements of a 7-stage ring oscillator.

capacitive loads for each stage of the ring oscillator. The 2-input NAND gate allowed the use of an enable signal to start or stop the oscillation (Fig. 7). The capacitive loads, which were unused transistor gates, allowed a crude frequency control demonstrating the feasibility of this method to control the speed of oscillation. At 40 V, without the capacitive loads, a maximum oscillation frequency of 2903 Hz was recorded, corresponding to a single-stage frequency of 40.6 kHz and a voltage controlled oscillator (VCO) gain of 131 Hz/V. With the capacitive loads the maximum oscillation frequency was reduced by 20% to 2297 Hz, a single-stage frequency of 32.2 kHz and a VCO gain of 103 Hz/V.

An alternative way to view the frequency variation would be 2600 ± 303 Hz (11.6%). Very often, it is important in circuit designs to be able to control the speed of a ring oscillator, for example, to meet external standards for data communication. However, wide process and fabrication tolerances, and varying operating conditions will cause the performance of sensitive circuits such as the ring oscillator to fluctuate greatly. By allowing the capacitive load at each ring oscillator stage to be variable and controllable, we will be able to regulate the ring oscillator to meet external specifications.

At 20 V, the oscillation frequencies with and without capacitive loads were measured as 424 Hz and 502 Hz, corresponding to single-stage frequencies of 5.94 kHz and 7.03 kHz respectively, a difference of 18.4%. The measured current for the inverter driving transistor at $V_{gs} = V_{ds} = 20$ V was 29.07 μA. The total capacitance seen by the output of a

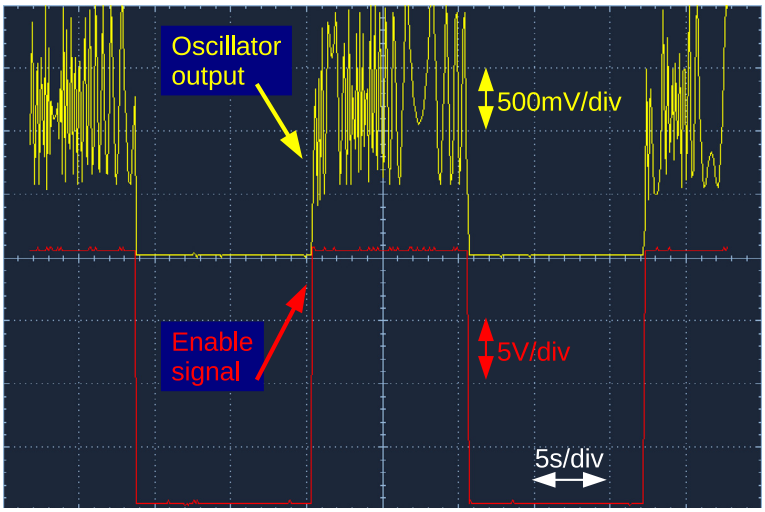


Fig. 7. 7-stage ring oscillator enable operation. Note that the start-up for an oscillator is unpredictable and that it took several seconds before stable oscillator operation.

ring oscillator inverter is estimated as 4.5pF. For a calculation of the rise or fall time of a ring oscillator inverter output, $t = CV/i$, where $C = 4.5$pF, $V = 20$ V, and $i = 14.54$ μA (average current). If we consider the diode-load transistor to be a constant current sink, this effectively reduces the charging current by the ratio of the transistor widths, i.e. a factor of 20, this gives a revised current $i = 13.81$ μA and a rise time $t = 6.5$ μs. The fall time is due entirely to the diode-load device, $i = 0.73$ μA, fall time = 123.8 μs. Adding rise and fall times gives a time period of 130.3 μs equivalent to a single-stage frequency of 7.7 kHz. The extra capacitive loads add an extra 2.25pF to every stage which results in a calculated single-stage frequency of 5.1 kHz, a difference of 50%. These calculations of the oscillation frequency are close to the measured results. Given the approximations made in the current values, the inverter's current profile while charging or discharging the load, and the difficulties associated with estimating the parasitic capacitances, the estimated frequencies are reasonable and give a first-order validation of the measured performance.

3.2. Memory

D-type flip-flops are an essential building block of a digital system. They allow the temporary storage, at clock speeds, of data while data is being processed at those same clock speeds. There are 2 styles of flip-flop design. The prevalent design for silicon CMOS circuits is based on back-to-back inverters and transmission gates [13]. However, for our unipolar process without complementary transistors, we decided to use a NAND-gate based design.

Normalised results and design schematics for the memory circuit are shown in Fig. 8. The design is a D-type flip-flop (DFF) of 93 printed wires but, for testability purposes, the inverting output is connected back to the input to make a T-type or toggle flip-flop which also shows that the flip-flop can be used without incurring a race condition. The expected function of a T-type flip-flop is that the output should toggle between high and low with each rising edge of input clock. The SPA was connected to the T-type flip-flop circuit providing power, clock and enabling monitoring of the non-inverting output. The clock period was approximately 6 s, and successful operation was measured at supply voltages of 10 V, 15 V and 20 V. At these supply voltages, the output high value is consistently at 95% of the supply voltage; 9.5 V, 14.25 V, 19 V respectively. This corresponds well with the diode-load nature of the logic design where the output high value is set by the ratios of the drive and load transistors [11]. The laminated E-Ink display was also shown to operate correctly at supply voltages of 27 V and 36 V. A video of the T-type flip-flop driving the E-Ink display is shown in the Supplementary information, video 1 (DFF-FIPS1).

3.3. Pass-code checker

By slightly altering the ink formulation, PEDOT:PSS resistors of different values can be printed [12] which were observed to be visually identical. With appropriately designed logic, it can be almost impossible to infer the precise circuit function from visual inspection only. One application which could make use of this observation is a pass-code checker which validates user input against a printed code. An implementation of a pass-code checker was completed with the addition of 4 printed touch sensors which could detect a finger-press (Fig. 1).

The touch sensors are 2 spirals of printed conductive silver wires (stylistically representing a fingerprint) which are shorted together when touched by a finger. The resistance of a finger was measured by a basic multimeter to be in the range 1–10 MΩ. In order to provide correct pull-up operation, much larger resistors of between 224 and 251 MΩ were printed. Other significantly smaller resistors 41–45 kΩ were also printed to demonstrate that 2 different values on the same substrate were possible.

The operation of the pass-code circuit is now explained, with reference to the circuit paths in Fig. 9. When a touch sensor is not being operated, the printed load resistors

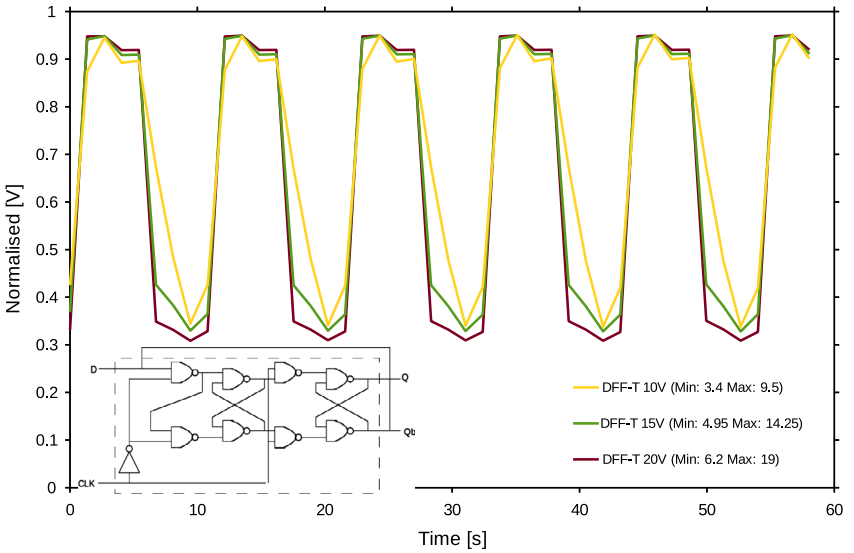


Fig. 8. Schematic (inset) and normalised measurements at different voltages of the Q output of a clocked D-flip-flop memory element constructed from 2-input NAND gates. The inverse output QB of the flip-flop has been connected back to the input to make a trigger-type flip-flop. The measurements are sampled and are not continuous time.

(224–251 MΩ) maintain nodes In2 and In4 at a logic-high level, measured at 19.8 V. Nodes In2 and In4 are connected to the input of separate inverters whose outputs, at nodes Mid2 and Mid4, are at a logic-low level, measured as 8.1 V and 6.5 V respectively. Mid2 and Mid4 in turn are connected to the gate of separate pull down transistors. The on-resistance of the pull-down transistors was measured to be approximately 3 MΩ at 20 V. The sources of the pull-down transistors, nodes Out2 and Out4, are further connected to printed pull-up pass-code resistors, 45 kΩ and 251 MΩ respectively. As node Out2 is connected to a small pull-up resistor value, then Out2 is easily pulled to a logic-high value of 19.9 V. Node Out4 is connected to a large pull-up value, so it is easily pulled to a logic-low value of 6.2 V. When the touch sensors are shorted by a finger press, it can be seen that Out2 does not change value and remains at a logic-high level. But node Out4 responds to the finger press by changing from a logic-low level to a logic-high level of 19.9 V.

The programming of the pass-code is easily accomplished by printing the desired resistor value as the pass-code resistor. In the example shown, pass-code resistors 2 and 3 are programmed as the pass-code. In order to activate the pass-code checker correctly, then touch sensors 2 and 3 must be operated. As mentioned previously, due to the visual similarities of the different valued printed resistors, it is almost impossible, by observation alone, to determine the correct touch sensor or pass-code resistor combinations to operate the pass-code checking circuit.

This simple pass-code circuit demonstrates the printing of different value resistors and the feasibility of touch operated switches.

3.4. Programmable array logic

The ring oscillator, memory element and pass-code checker were all implemented on the first FIPS1 foil which had a programmable array architecture of 54 uncommitted transistors. Although in principle straightforward, it proved extremely difficult and time consuming to implement larger, more intricate circuit designs due to the limited single layer interconnect capacity and a restriction to designing at transistor level. For the second foil FIPS2, a PAL (Fig. 10) with extensive routing capabilities by a programmable switch fabric was designed featuring 8 inputs, 8 outputs, 32 product terms, a fully programmable AND-plane, a fixed OR-plane, and a programmable macrocell at every output with memory, true and inverse output options. Although the inkjet printing is still only a single layer of silver wires, when compared to the FIPS1 array architecture, the routing capacity on the FIPS2 array architecture is increased greatly when augmented by the switch fabric that makes use of all 3 metal mask layers.

To demonstrate a design on the PAL, a 2:4 demultiplexer directly driving the E-Ink display was implemented. The demultiplexer is a combinatorial logic circuit which decodes two inputs in order to drive one of the three E-Ink display patterns, or none of them. The other PAL inputs and outputs were unused and not connected. With reference to Fig. 10 and Table 1, the 2:4 demonstrator logic was implemented as follows:-

$$Y0 = I0.I1\ (Vine\,pattern)$$
$$Y1 = I0.\bar{I1}\ (Swirl\,pattern)$$
$$Y2 = \bar{I0}.I1\ (Background\,pattern)$$

Part of the inkjet printed programming connections are shown in the micrograph, Fig. 3. Silver wires were also inkjet printed to the edge of the foil to provide connection points for the inputs, power and display common node. These connection points were attached to external wires by silver dag and secured with glue. Measurements of the E-Ink driving voltages for a 20 V supply voltage were in the range 16.7–18.9 V. For a portable demonstrator, the

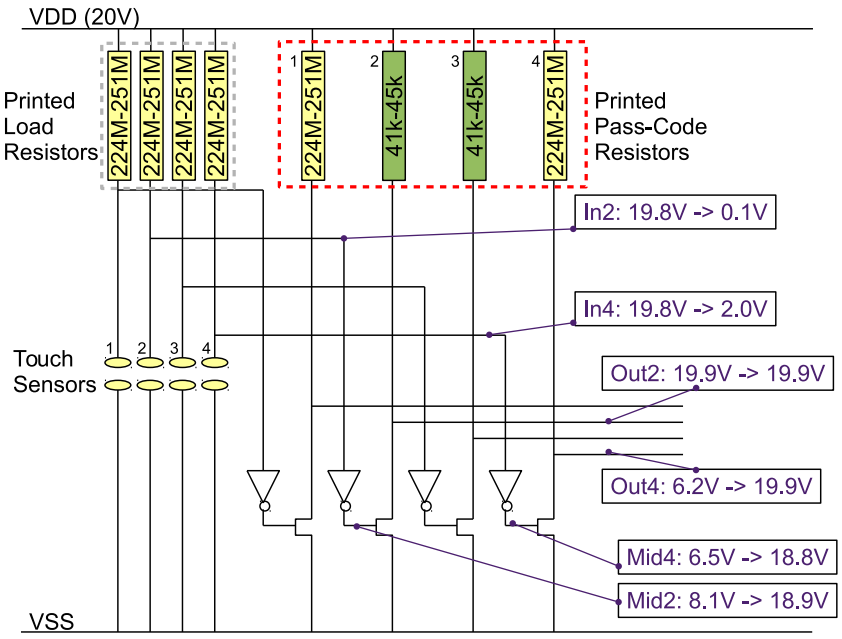


Fig. 9. Schematic of the pass-code checker circuit which contains different values of printed PEDOT:PSS resistors, printed touch sensors, and transistors. The values shown at the indicated nodes represent measured voltage values for 'finger-off' to 'finger-on' operation.

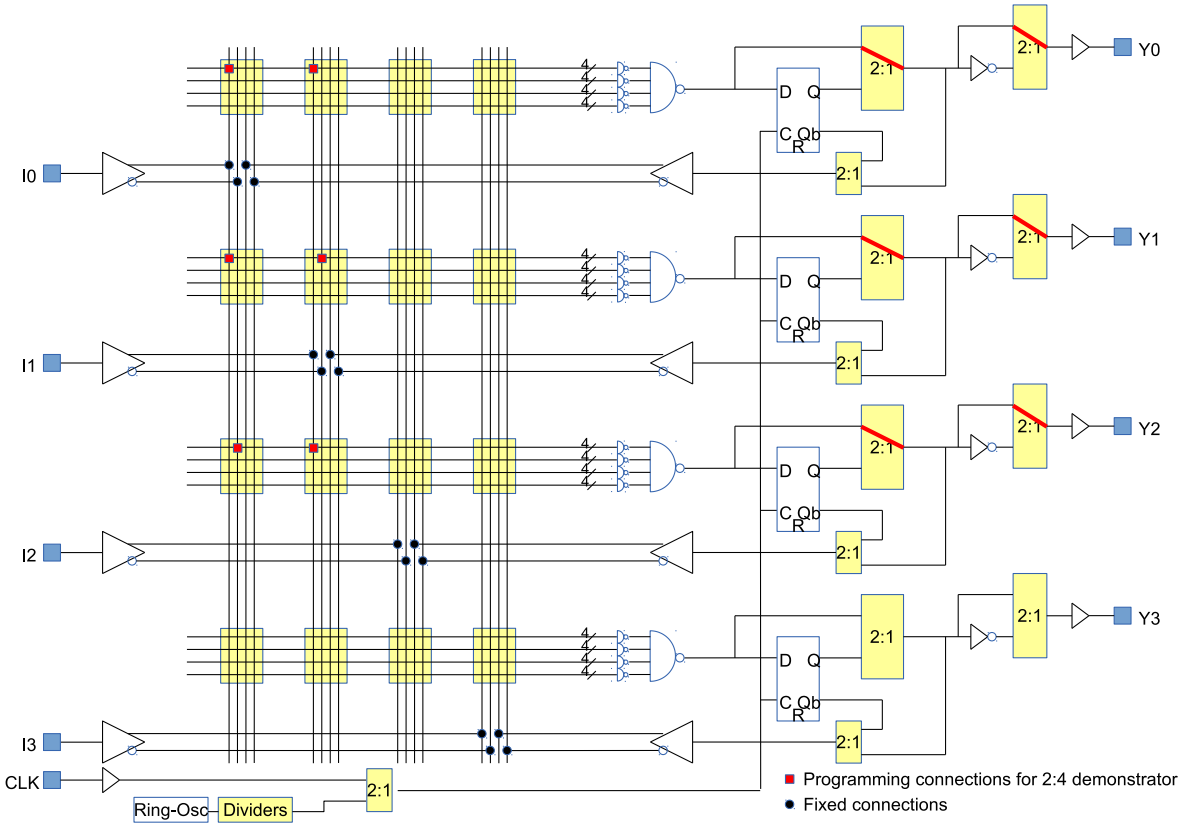


Fig. 10. Simplified schematic of part of the PAL showing the programming connections for the 2:4 demultiplexer demonstrator. The yellow boxes represent inkjet programmable areas of the switch fabric. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

Table 1
Demultiplexer function truth table.

I0	I1	Vines	Swirls	Background
0	0	0	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

external supply wires were connected to four 9 V PP3 batteries providing a total 36 V. The E-Ink common external wire was attached to the 27 V point of the four batteries and the inputs alternately touched on the 0 V or 36 V terminals as necessary to provide logical input to the demultiplexer. This portable demonstrator was shown to work on the desktop with no external components other than the four batteries. For practical applications, it will be necessary to operate at much lower voltage levels. 36 V was chosen because it provided the best display performance for the demonstration. As we saw from the memory circuit previously, operation is viable down to 10 V but this would have led to a degraded display, both in terms of the speed of black/white switching and in black/white intensity. Retesting of the portable demonstrator after 9 months storage in normal office conditions showed that the 2:4 demultiplexer circuit and display were still fully functional. A video of the demultiplexer operation is provided in the Supplementary information, video 2 (Demux-FIPS2).

4. Conclusions

In this work we have demonstrated the first examples of programmable arrays of logic devices with organic devices programmed by the inkjet printing of conductive silver wires and PEDOT:PSS resistors. We have also demonstrated an organic transistor circuit driving a flexible display integrated on a single PEN substrate, the only external components being batteries.

Demonstrating the synergy between inkjet printing as an additive processing step and organic device fabrication, this work further validates the concept of inkjet programmable, flexible organic devices with displays being used for rapid circuit prototyping. Programmable devices realise valuable time and cost savings in the design and fabrication of complex circuits by allowing end users to share a common platform which can be customised quickly and reliably. Moreover, the programmable arrays of logic devices are fabricated using Plastic Logic's uniform active matrix transistor array process for displays which is already fully industrialised, and proven to be high yielding and reliable. Furthermore, it is expected that by extending this work with larger digital designs and incorporating analogue circuit elements, flexible organic electronic subsystems will be ideally placed for markets that are currently served by conventional, though bulky, discrete printed circuit boards but are too small for custom designed integrated silicon chips.

Acknowledgements

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Appendix A. Supplementary material

Supplementary data associated with this article can be found, in the online version, at http://dx.doi.org/10.1016/j.orgel.2014.08.032.

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