This Accepted Manuscript is available for reuse under a CC BY-NC-ND licence after the 12 month embargo period provided that all the terms of the licence are adhered to. The published manuscript (Luis Portilla *et al* 2021 *Nano Futures* **5** 025001) is available at https://doi.org/10.1088/2399-1984/abf6b1.

Ambipolar Carbon Nanotube Transistors with Hybrid Nanodielectric for Low-Voltage CMOS-like Electronics

Authors: Luis Portilla[1,2], Jianwen Zhao[2*], Jing Zhao[1], Luigi. G. Occhipinti[3], Vincenzo Pecunia[1*]

Affiliations

[1]Jiangsu Key Laboratory for Carbon-Based Functional Materials & Devices, Institute of Functional Nano & Soft Materials (FUNSOM), Joint International Research Laboratory of Carbon-Based Functional Materials and Devices, Soochow University, 199 Ren'ai Road, Suzhou, 215123 Jiangsu, China.

[2]Printable Electronics Research Centre, Suzhou Institute of Nanotech and Nano-bionics, Chinese Academy of Sciences, No. 398 Ruoshui Road, SEID, Suzhou Industrial Park, Suzhou, Jiangsu Province, 215123, China.

[3]Department of Engineering, University of Cambridge, 9 JJ Thomson Avenue, Cambridge CB3 0FA, United Kingdom.

*Correspondence to: jwzhao2011@sinano.ac.cn (Jianwen Zhao); vp293@suda.edu.cn (Vincenzo Pecunia).

Abstract

The proliferation of place-and-forget devices driven by the exponentially-growing Internet of Things industry has created a demand for low-voltage thin-film-transistor (TFT) electronics based on solution-processible semiconductors. Amongst solution-processible technologies, TFTs based on semiconducting single-walled carbon nanotubes (sc-SWCNTs) are a promising candidate owing to their comparatively high current driving capability in their above-threshold region at low voltages, which is desirable for applications with constraints on supply voltage and switching speed. Low-voltage above-threshold operation in sc-SWCNTs is customarily achieved by using high-capacitance-density gate dielectrics such as metal-oxides fabricated via atomic layer deposition (ALD) and ion-gels. These are unattractive, as ALD requires complex-processing or exotic precursors, while ion-gels lead to slower devices with poor stability. This work demonstrates the fabrication of low-voltage above-threshold sc-SWCNTs TFTs based on a high-capacitance-density hybrid nanodielectric, which is composed of a readily-made AlO_x nanolayer and a solution-processed self-assembled monolayer (SAM). The resultant TFTs can withstand a gate-channel voltage of 1–2 V, which ensures their above-threshold operation with balanced ambipolar behavior and electron/hole mobilities of 7 $cm^2V^{-1}s^{-1}$. Key to achieving balanced ambipolarity is the mitigation of environmental factors via the encapsulation of the devices with an optimized spin-on polymer coating, which preserves the inherent properties of the sc-SWCNTs. Such balanced ambipolarity enables the direct implementation of CMOS-like circuit configurations without the use of additional dopants, semiconductors or source/drain electrode metals. The resultant CMOS-like inverters operate in the above-threshold region with supply voltages in the 1–2 V range, and have positive noise margins, gain values surpassing 80 V/V, and

Accepted Manuscript

a bandwidth exceeding 100 kHz. This reinforces SAM-based nanodielectrics as an attractive route to easy-to-fabricate sc-SWCNT TFTs that can operate in the above-threshold region and that can meet the demand for low-voltage TFT electronics requiring moderate speeds and higher driving currents for wearables and sensing applications.

1. Introduction

Low-temperature solution-processed electronic materials are key to the development of soft-electronics (e.g. flexible, stretchable, plastic, etc.), due to their versatility and ease of deposition over large areas using additive, on-demand techniques such as printing and coating [1–4]. The adaptability of these materials to such techniques has enabled and motivated a manifold of printed electronic and optoelectronic applications [5–9]. Among low-temperature solution-processed semiconductors, semiconducting single-walled carbon nanotubes (sc-SWCNTs) are highly promising for high-performance thin-film transistors (TFTs), especially in view of their comparatively high field-effect mobility and low threshold voltages (V_T) [10–13]. Solution-deposited/printed sc-SWCNTs can form a random network (sc-SWCNTN), which results in a robust semiconducting layer that has been implemented in a myriad of hard and/or soft electronics, such as microprocessors [14–16], storage devices [17], flexible integrated circuits [18], sensing devices for the Internet of Things (IoT) [19,20], biosensors [21,22], and wearable electronics [23,24]. In particular, the realization of low-voltage TFT electronics with moderate switching speeds (> 1kHz) is of fundamental importance for off-the-grid applications where specific sampling rates or faster reaction times may be required, as could be the case in wearable electronics and remote sensing applications. It is important to consider that the power supply available in off-the-grid scenarios may consist of a compact energy harvester or a flexible battery, which can only provide limited supply voltages (of the order of 1 V) [25–28]. Therefore, to address applications with constraints on both supply voltage and switching speed, it is important to develop easy-to-fabricate TFT electronics that can operate at low voltage (< 2 V) in the above-threshold region (power supply voltage greater than V_T). Indeed, above-threshold operation guarantees the full current driving capability for a given semiconductor technology, which is conducive to higher switching speeds. Additionally, above-threshold low-voltage operation is also desirable for the driving of other electronic devices, which may require high currents, such as light emitting diodes, radio frequency components, etc. Therefore, the pursuit of a versatile/easy-to-process approach to sc-SWCNTN TFTs for the realization of low-voltage above-threshold electronics is a high priority [3,19,29,30].

Low-voltage above-threshold operation in sc-SWCNTN TFTs has been achieved to date by boosting the gate-to-channel capacitive coupling with particularly thin gate dielectric layers and/or gate dielectric materials with high relative permittivity (high-κ) [31,32]. In this regard, a widely reported approach involves the atomic layer deposition (ALD) of ~10-nm-thick layers of high-κ materials (e.g. Al_2O_3, HfO_2). However, ALD suffers from a complex process, slow throughput and also tends to involve higher temperatures (≥ 200 °C) and exotic precursors [33–35]. Similarly, ion-gels have often been employed to realize low-voltage sc-SWCNTN TFTs because of their very high capacitance densities and their ease of deposition by printing. However, the resulting devices suffer from poor chemical/electrical stability and from very high parasitic capacitance, which, in turn, limits the TFT switching speed [29,36–39]. An attractive strategy that would in principle overcome the limitations of the aforementioned mainstream approaches would involve the use of a SAM nanodielectrics, an approach that we have recently demonstrated to be viable in the deep-

Accepted Manuscript

subthreshold region [31]. Such a gate dielectric has a total thickness of ~5 nm, and comprises a ~2-nm-thick self-assembled monolayer (SAM) grafted atop the ~3 nm oxide of a gate electrode (e.g., made of aluminum) [31,40,41], thereby enabling a high capacitance density. On one hand, such nanodielectrics are particularly easy to fabricate, as they require the solution-based deposition of a SAM onto the nm-thick oxide of a gate electrode (cf. ALD dielectrics). Moreover, a wide range of SAM nanodielectrics are chemically inert and allow excellent device stability (cf. ion-gel dielectrics) [42,43]. In fact, the attractiveness of hybrid SAM-based nanodielectrics has determined their extensive use in organic thin-film transistors (OTFTs) since their introduction in 2007 by Halik, Klauk et al. [40,41,44]. Interestingly, this kind of nanodielectric layer had not been investigated in sc-SWCNTN TFTs until our recent work on deep-subthreshold sc-SWCNTN electronics, where we reported on its use for TFT operation in the deep-subthreshold region, i.e., at voltages much less than V_T (V_{DD} = 0.2 – 0.5 V) [31]. However, the ability of such dielectrics to withstand voltages large enough (≥ 1 V) to deliver above-threshold sc-SWCNTN TFTs and circuits has not been reported to date. Importantly, the closest work on above-threshold sc-SWCNTNs TFTs that relies on a hybrid SAM-based dielectric, by Schießl *et al.*, involves the ALD deposition of a 4-nm-thick oxide layer followed by its capping with a variety of SAM molecules, and therefore involves the complex processing associated with ALD, and additionally results in devices with large hysteresis and unipolar (p-channel) characteristics (i.e., preventing robust circuit integration via CMOS/CMOS-like strategies) [35].

In this work, we demonstrate low-voltage ambipolar TFTs and CMOS-like electronics operating at voltage values above the V_T based on sc-SWCNTNs printed atop an easy-to-fabricate SAM/aluminum-oxide hybrid nanodielectric. Specifically, we use such hybrid-nanodielectric approach as a platform for the realization of TFTs with well-balanced above-threshold ambipolar characteristics, thanks to the concurrent adoption of an optimized spin-on polymer encapsulation layer. The entirety of the process involves a low temperature budget (≤ 120 °C) and primarily relies on solution-based steps (for the deposition of the SAM nanodielectric, semiconductor, and encapsulant), which makes it potentially attractive for developing electronics on low-cost, flexible or stretchable substrates. To demonstrate the applicability of the fabricated ambipolar sc-SWCNTN TFTs to CMOS-like circuits, we realize CMOS-like inverters and characterize their static and dynamic characteristics at operating voltages up to 2 V, resulting in more favorable gains and switching speeds compared to gates operating exclusively in the deep-subthreshold region [31]. The well-conditioned characteristics of these inverters reinforce the case for the adoption of SAM nanodielectrics—which have a simpler fabrication process than ALD dielectrics and better stability than ion-gels—to fabricate low-voltage ambipolar sc-SWCNTN TFTs compatible with the supply voltage constraints of emerging off-the-grid applications requiring moderate speeds and/or higher current driving capability.

2. Materials and methods

2.1 Materials

All chemicals and reagents were used as received without further refinement. The solvents toluene (CAS: 108-88-3), trifluorotoluene (CAS: 98-08-8), 2-propanol (CAS: 67-63-0), n-butyl acetate (CAS: 123-86-4) and n-methyl-2-pyrrolidone (NMP) (CAS: 872-50-4) used for device fabrication were purchased from Sigma Aldrich. The organic molecule n-octadecylphosphonic acid (C_{18}-PA) and the polymer poly(methyl methacrylate) (PMMA) ($M_W \approx 120{,}000$) (CAS: 9011-14-7) were

Accepted Manuscript

bought from Sigma Aldrich. CYTOP and its solvent CT-SOLV180 were purchased from Asahi Glass Co. Ltd. P(VDF-TrFE-CFE) was procured from Piezotech Arkema-CRRA. The photoresist S1813 and the resist LOR5B were purchased from Microchem-Kayaku Advanced Materials. The isoindigo-based polymer poly(9, 9-dioctylfluorene) (PFO) derivative (PFIID) was synthesized in-house as described in a recent report [45]. Finally, the P2 arc discharge single-walled carbon nanotubes (SWCNTs) were purchased from Carbon Solutions.

2.2 Synthesis of semiconducting sc-SWCNT ink

The semiconducting ink was prepared by mixing in a glass vial 5 mg of PFIID polymer and 10 mg of SWCNTs and 20 mL of toluene [46]. The mixture was successively subjected to an ultrasonication process for 30 minutes at 0 °C with VCX 130 (60 W) (Sonics & Materials Inc., USA). To remove any insoluble materials, the sonicated mix was centrifuged at 30000×g for 2 h, after which the supernatant was meticulously extracted with a pipette resulting in the sc-SWCNT ink. The ink was confirmed to consist of only sc-SWCNTs via UV-Vis-NIR spectroscopy with a Lambda 750 UV-Vis-NIR (Perkin Elmer, USA) [37]. The ink was then diluted by adding toluene until a maximum absorbance of 0.35 of the semiconducting peaks (800-1200 nm) was obtained in a quartz cuvette with a total optical path of 10 mm [37]. This concentration resulted in functional devices as described herein using a single printing pass. Afterwards, half of the solvent was removed by applying a mild negative air pressure within a chemical hood and the evaporated solvent was replaced with trifluorotoluene resulting in an ink with a 1:1 volume ratio of toluene:trifluorotoluene. The solvent mixture had no effect in the homogeneity of the ink. Lastly, 50 µL of terpinol per mL of ink was added to the ink in order to ease mist generation as required by the aerosol-jet printing process.

2.3 SAM Solution Preparation

The solution for SAM deposition was realized by mixing in a sealed glass vial 2.0 mg of the C_{18}-PA molecule with 30 mL of 2-propanol. The C_{18}-PA molecule was fully solubilized, yielding a transparent solution with the aid of no less than 15 minutes of ultrasonication in a water bath.

2.4 Fabrication of thin-film transistors and inverter gates

2.4.1 Al gate and SAM-based nanodielectric

Bare glass substrates were washed thoroughly in 2-propanol with the aid of an ultrasonic bath. The substrates were sonicated for at least 5 minutes and were subsequently dried with dry nitrogen gas. 30-nm-thick high-purity (99.99%) Al gate electrodes were thermally evaporated in high vacuum (pressure < 2.0×10^{-6} mbar) through a shadow mask onto the bare glass substrate. Subsequently, the patterned Al gates were exposed to an oxygen plasma treatment for 5 minutes in an oxygen atmosphere of 0.2 mbar at 140 W for 5 minutes [31,41]. Finally, a SAM consisting of C_{18}-PA was formed atop the AlO_x layer by immersing the substrate for not less than 16 hours in the C_{18}-PA SAM solution. The substrate was then rinsed with pure 2-propanol so as to remove any unbound SAM molecules. This was followed by a drying process using pressurized nitrogen. Finally, samples were annealed for 5 minutes at 70 °C in order to eliminate any remaining 2-propanol on the sample surface.

Accepted Manuscript

2.4.2 Printing of the sc-SWCNTN

The sc-SWCNTN was fabricated by depositing the sc-SWCNT ink on the Al/AlO_x/SAM stack through aerosol-jet printing (Optomec, USA). The printing speed was set to 1.5 mm/s. After printing, the samples were annealed at a temperature of 120 °C for 10 minutes in environmental conditions to remove remaining solvent and aid in the surface immobilization of the sc-SWCNTs. Then, the substrate was rinsed with pure toluene in order to remove any excess PFIID polymer and sc-SWCNTs. Finally, the samples were dried with pressurized nitrogen and annealed again at 120 °C in air for 10 minutes to remove the remaining toluene.

2.4.3 Au source and drain electrodes

The fabrication of the source and drain electrodes was carried out using a standard double-layer lift-off photolithography (based on LOR5B and S1813 resists) [47]. The deposition of the 30 nm thick high purity (99.99%) Au source and drain electrodes was conducted via thermal evaporation in high vacuum (pressure < 2.0×10^{-6} mbar). The resist lift-off procedure was performed by immersing the samples for 30 minutes in NMP, followed by rinsing in 2-propanol, drying with pressurized nitrogen gas, and annealing for 5 minutes at 70 °C.

2.4.4 Encapsulation

Samples were first annealed on a hotplate (120 °C for 3 h) within a nitrogen-filled glovebox. Then, the samples were coated with a layer or bi-layer of polymers consisting of: 1) a single 180-nm-thick PMMA layer; 2) a single 800-nm-thick PMMA layer; 3) a bi-layer consisting of a 180-nm-thick PMMA layer and 1000-nm-thick P(VDF-TrFE-CFE) layer; 4) a bi-layer consisting of a 180-nm-thick PMMA layer and a 500-nm-thick CYTOP layer. The layers were deposited via spin coating (2000 rpm) within a nitrogen-filled glove box. For the bi-layers, the PMMA layer was spin coated first. After spin coating the PMMA layer, the samples were annealed for 30 min at 90 °C within a glovebox. The P(VDF-TrFE-CFE) or CYTOP layer was spin coated afterwards (2000 rpm) and the substrate was annealed at 60 °C or 90 °C respectively for 30 minutes. The PMMA solutions were n-butyl acetate based with a concentration of 40 g/L (resulting in a 180-nm-thick layer) or 80 g/L (resulting in an 800-nm-thick layer). P(VDF-TrFE-CFE) was dissolved in n-butyl acetate at a concentration of 80 g/L. The CYTOP polymer was received in solution and the spin coating solution consisted of one part CYTOP (as received) and two parts CT-SOLV180.

2.5 Capacitor fabrication

Capacitors with an area of 50×50 µm were fabricated to determine the capacitance density of the fabricated hybrid nanodielectric. The bottom electrode was fabricated as described in section 2.4.1 with the exception that a different shadow mask was used in this case. The capacitor top electrode was fabricated via thermal evaporation of 30 nm of high purity (99.99%) Au in high vacuum (pressure < 2.0×10^{-6} mbar) via a shadow mask.

2.6 Electrical Characterization

The electrical characterization of devices was performed using shielded micromanipulator probes on a grounded probe station under environmental and dark conditions. A semiconductor parameter analyzer (Keithley 4200A, Keithley Instruments, USA) was used to obtain the transfer and output characteristics of the TFTs, the breakdown voltage and current leakage of the dielectric, and the

Accepted Manuscript

voltage transfer characteristics (VTCs) of the inverters. Signal generator and oscilloscope measurements were conducted with a Picoscope 3000 (Pico Technology, U.K.). The impedance/capacitance measurements were conducted with a Hioki IM3533 LCR meter (Hioki, Japan). All electrical measurements were conducted as soon as the last step of their corresponding fabrication process was completed.

2.7 XPS analysis

The X-ray photoelectron spectroscopy (XPS) measurements were conducted with a Kratos Axis Ultra^{DLD} spectrometer (Kratos Analytical Limited) employing an Al Kα source (1486.6 eV). The take-off angle was 90°, the pass energy was 20 eV with a step size of 0.1 eV, and the analysis area was 700×300 μm. The XPS samples were prepared as specified in section 2.4.1.

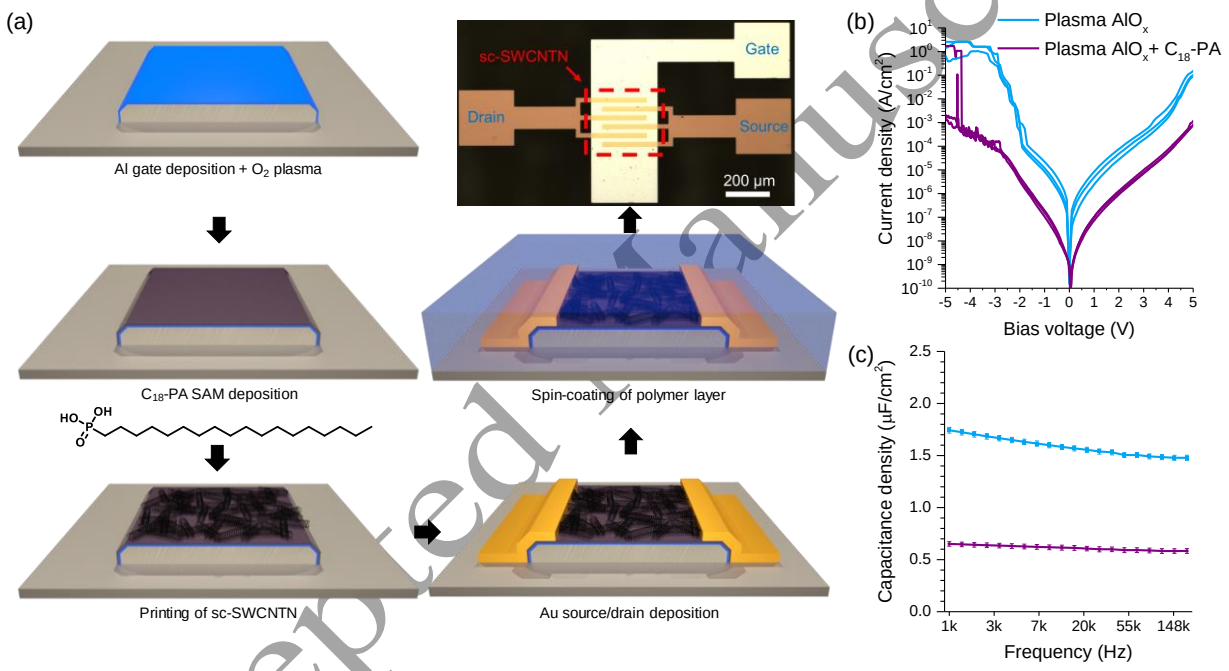

Fig. 1. (a) Process steps for the fabrication of sc-SWCNTN TFTs and a top-view micrograph of a complete TFT. (b) Measured areal capacitance and (c) leakage current density of 50×50 μm^2 capacitors consisting of either an AlO_x nanodielectric or an AlO_x + C_{18}-PA hybrid-nanodielectric.

3. Results and discussion

The TFTs we explored rely on the bottom-gate top-contact architecture, and their fabrication consists of five steps, as depicted in **Fig. 1a**. The process begins with the deposition of the Al gate electrode, which is then subjected to a commonplace oxygen plasma surface-cleaning step, which also consolidates the nm-thick native AlO_x overlayer inherently covering the Al gate electrodes upon exposure to air. The thickness of the resultant AlO_x overlayer was 3.4 nm, as determined via X-ray photoelectron spectroscopy (XPS) (SI1). Such an AlO_x layer is not sufficiently robust for use as a standalone gate dielectric, owing to its high leakage current (**Fig. 1b**). In order to tackle this issue, we cap the AlO_x layer with a self-assembled monolayer (SAM) based on a

Accepted manuscript

commercially-available n-octadecylphosphonic acid (C_{18}-PA). The SAM deposition involves a facile solution-based step, consisting in the immersion of the sample in a solution of SAM molecules. The resultant hybrid dielectric is considerably more robust, giving a leakage current density below 1 μA/cm^2 at 1 V (**Fig. 1b**). This improvement arises from an effective full surface coverage of the C_{18}-PA SAM onto the AlO_x layer, as determined with impedance spectroscopy (SI2). Due to its overall nm-scale thickness, the hybrid nanodielectric delivers a high capacitance density of around 0.65 μF/cm^2 at 1 kHz (**Fig. 1c**). Such a hybrid nanodielectric is attractive for the realization of low-voltage TFTs. In fact, a gate dielectric with high capacitance density C_{ox} would enable steep subthreshold swings (SS) according to **Equation 1**:

$$SS = \frac{1}{\log_{10}(e)} \frac{kT}{q} \left(1 + \frac{D_{tr}q}{C_{ox}}\right) \qquad (1)$$

Here, q is the elementary charge, k is the Boltzmann constant, T the absolute temperature, D_{tr} the interfacial trap density, and C_{OX} the areal capacitance of the dielectric. In turn, a steep subthreshold slope reduces the magnitude of the gate voltage that needs to be applied to accumulate charge carriers in a TFT channel, hence enabling low-voltage operation [48]. After the deposition of the hybrid nanodielectric, the TFT active layer (sc-SWCNTN) is additively deposited via aerosol-jet printing (AJP) over a region with an area of 350×350 μm^2 overlapping the gate electrode, as depicted in **Fig. 1a**. Finally, Au source and drain electrodes are fabricated atop the sc-SWCNTN, followed by the coating of the TFT stack with a polymer bi-layer (PMMA/CYTOP) (see Section 2.4.4), which serves as an encapsulation.

The resulting encapsulated TFTs can be fully switched 'on' at gate voltages of less than 2 V, manifesting an ambipolar behavior, as is evident from the measured transfer and output characteristics depicted in **Fig. 2a-b**. **Fig. 2a** clearly demonstrates the TFT ambipolarity, because, as the gate voltage is swept from positive to negative, there is firstly a dip and then a rise in the channel current. This reflects a transition from an electron current (for positive gate voltages of sufficiently large magnitude) to a hole current (for negative gate voltages of sufficiently large magnitude). In particular, the encapsulated devices exhibit well-balanced ambipolar characteristics, as exemplified by the symmetry of the transfer curve shown in **Fig. 2a,** and by the closely-matching magnitudes of the channel current in the *n*-channel and *p*-channel accumulation regions in the output curves in **Fig. 2b**. In contrast, having the semiconducting layer exposed to environmental conditions (no encapsulation) results in the TFTs exhibiting a dominant *p*-channel behavior, higher drain currents in hole accumulation (**Fig. 2c-d**), and a more pronounced hysteresis in the *n*-channel region (**Fig. 2c**). The *p*-channel character and pronouncedly hysteretic behavior of the non-encapsulated devices is expected to arise from the influence of oxygen and/or water on the sc-SWCNTN [49,50]. Moreover, in addition to well-balanced characteristics, the encapsulated devices (as compared to the non-encapsulated ones) have an all-around better ambipolar performance with higher on/off ratios and steeper SS values, which arise from a reduced trap state density (**Table 1**). This is likely determined by the lack of exposure of the active layer to environmental species [51]. The average performance parameters (such as mobility, on/off ratio, V_T, SS and trap density) of the sc-SWCNTN TFTs before and after encapsulation are summarized in **Table 1** (SI3, SI4).

The encapsulated TFTs discussed up to this point feature a PMMA/CYTOP encapsulation stack, as we determined that this provides superior barrier properties. To reach this conclusion, we compared three spin-on polymeric encapsulants (**Fig. 3a**) in the following configurations: a) a 180-nm-thick PMMA film; b) an 800-nm-thick PMMA film; c) a 1000-nm-thick P(VDF-TrFE-CFE)

Accepted Manuscript

film stacked on top of a 180-nm-thick PMMA film; d) a 500-nm-thick CYTOP film stacked on top of a 180-nm-thick PMMA film. The choice of having the same polymer (PMMA) in direct contact with the sc-SWCNTN is motivated by our interest in ascertaining which encapsulation scheme is more resilient to environmental species while ruling out the effects of the encapsulant chemistry. In fact, previous studies have proposed that the chemistry of the encapsulant in direct contact with a sc-SWCNTN can have an impact on sc-SWCNTN TFT characteristics [52]. The resultant transfer curves with the different encapsulant configurations—measured directly after the encapsulation process—are shown in **Fig. 3b**. To understand these results, it is useful to consider the zero transconductance points (ZTPs) of these current-voltage curves, which correspond to the V_{GS} values at which the drain current is lowest. Indeed, the ZTP acts as a convenient indicator of how *n*-channel compares to *p*-channel conduction, granted that the semiconductor exhibits comparable *n*-channel and *p*-channel intrinsic mobilities (as is the case for sc-SWCNTs).

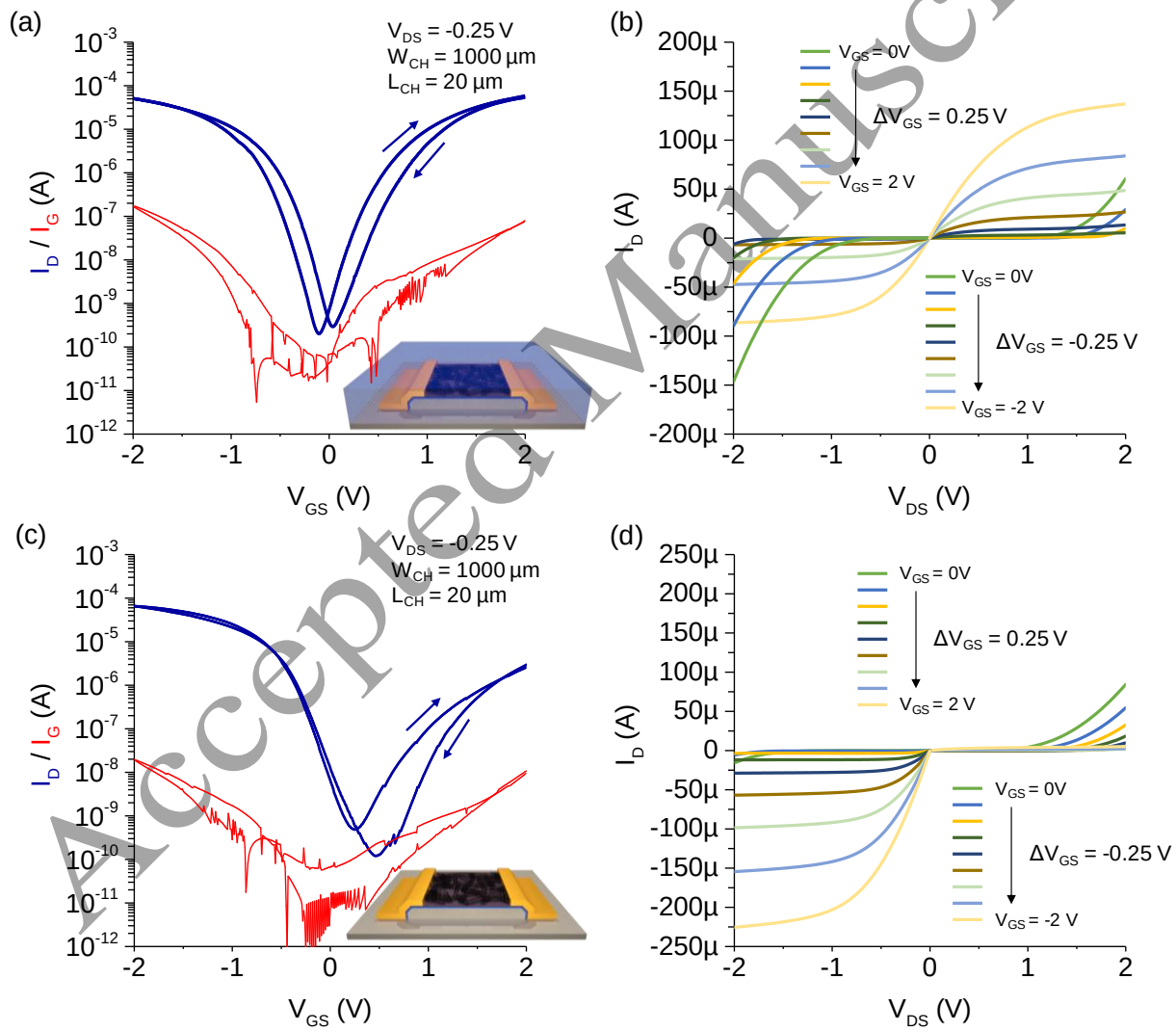

Fig. 2. Device characteristics. (a) Transfer and (b) output characteristics of a sc-SWCNTN TFT encapsulated with PMMA/CYTOP. (c) Transfer and (b) output characteristics of a non-encapsulated sc-SWCNTN TFT (i.e., a TFT having the active layer exposed to the environment). The gate leakage current difference in (a) and (c) are due to device to device variations

Accepted Manuscript

Table 1
Performance parameters of six sc-SWCNTN TFTs with and without PMMA/CTYOP encapsulation (measured in air).

	Non-encapsulated		Encapsulated	
	n-channel	*p*-channel	*n*-channel	*p*-channel
Mobility ($cm^2\ V^{-1}\ s^{-1}$)	1.2 ± 0.3	7.6 ± 1.6	8.2 ± 1.8	6.7 ± 1.7
On/Off ratio	≈ 3.5	≈ 5	≈ 5.3	≈ 5.3
V_T (V)	1.48 ± 0.03	-0.48 ± 0.04	1.07 ± 0.11	-0.89 ± 0.09
Subthreshold swing (mV/decade)	282 ± 24	-227 ± 35	185 ± 21	-155 ± 15
Trap density ($10^{12}\ eV^{-1}\ cm^{-2}$)	15.8	11.9	8.9	6.86

Essentially, a ZTP that is further to the right along the V_{GS}-axis, corresponds to a situation in which the encapsulation layer provides smaller protection of the sc-SWCNTNs against environmental species. This is consistent with the dominance of *p*-channel conduction and the large ZTP observed in sc-SWCNTN TFTs without any encapsulation (**Fig. 2**), and is in agreement with relevant literature [49,50]. Based on this metric, we observe that the 180-nm-thick PMMA layer is the most ineffective encapsulant among the configurations considered herein, as the corresponding devices exhibit the largest positive ZTP (**Fig. 3b**). Similarly, thicker PMMA layers (800 nm) prove to be more effective, but the corresponding ZTP is still comparatively close to the one obtained with a thinner PMMA encapsulation. In the case of the PMMA/P(VDF-TrFE-CFE) encapsulation, an intermediate ZTP among the configurations considered herein is observed. We attribute this effect to the fact that the PMMA/P(VDF-TrFE-CFE) stack corresponds to the encapsulation layer with the largest overall thickness (≈ 1000 nm), while the polar nature of its P(VDF-TrFE-CFE) component is detrimental to its barrier properties against moisture. In contrast, it is evident that the PMMA/CYTOP stack provides superior barrier properties with respect to ambient species, as the ZTP of the corresponding TFTs is the furthest to the left along the V_{GS}-axis among the configurations considered herein. We attribute this to the better barrier properties of CYTOP, owing to its superior hydrophobicity compared to the other polymers employed [53–55]. Considering that devices encapsulated with PMMA/CYTOP offer the most ideal ambipolar characteristics, we adopted PMMA/CYTOP as the encapsulation of choice in all subsequent experiments.

As our approach preserves the intrinsic balanced sc-SWCNTN ambipolarity, we pursued the integration of the encapsulated sc-SWCNTN TFTs into digital inverter gates. Specifically, we adopted a CMOS-like configuration [56], with the inverters comprising two nominally identical TFTs connected as shown in **Fig. 4a-b**. Crucially, this approach builds on the fact that our TFTs deliver similar current levels for symmetric gate voltage values, thanks to their well-conditioned ambipolar characteristics. The resultant CMOS-like inverters deliver favorable noise margins NM > 0 V, as evident from **Fig. 4b-c** (see also **Table 2**). Additionally, the inverters have a particularly high gain of up to 86 V/V, good rail-to-rail values and switching thresholds near $V_{DD}/2$. Such performance is well aligned with the requirements for the fabrication of more complex digital circuits [57]. By contrast, the non-encapsulated devices are unsuitable for CMOS-like integration (**Fig. 4d**), because the current disparity between their *n*- and *p*-channel regions amounts to almost two orders of magnitude (**Figure 2c**). In fact, the resulting noise margins are negative or exceedingly small (SI5), fundamentally barring the use of the non-encapsulated devices in digital circuits.

Accepted Manuscript

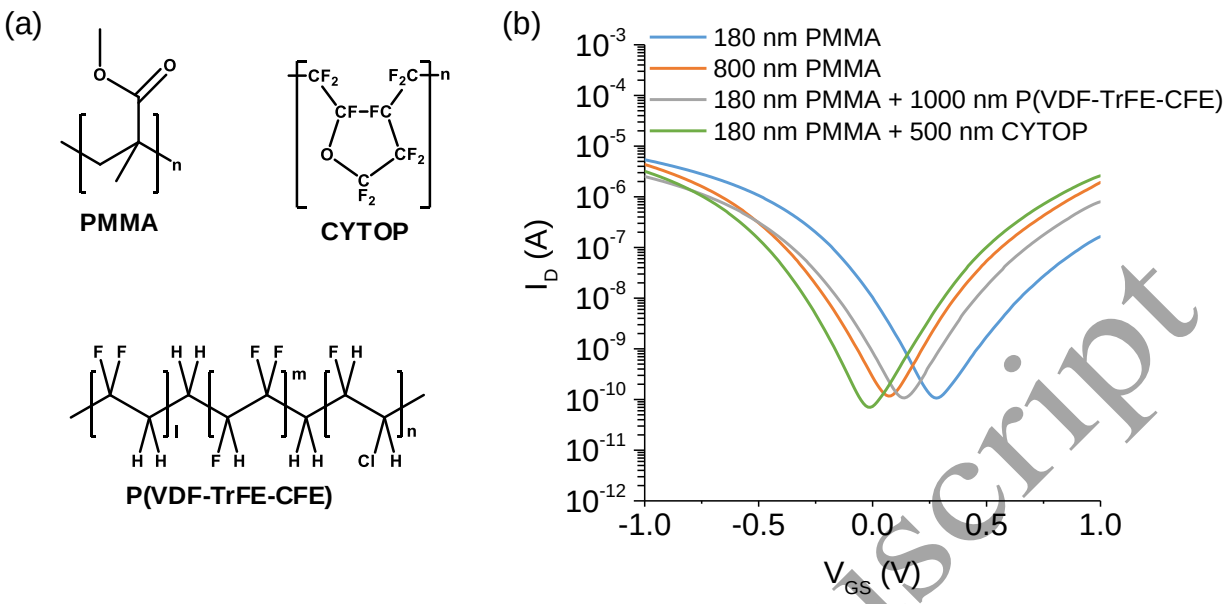

Fig. 3. Encapsulation materials. (a) Molecular structures of the polymers employed for the encapsulation of the sc-SWCNTN TFTs. (b) Transfer characteristics of sc-SWCNTN TFTs with different encapsulation stacks.

To assess the switching speed of the hybrid-nanodielectric-based inverters featuring a PMMA/CYTOP encapsulation, we characterized their response to a 1 kHz square wave signal at the input terminal. The resulting waveforms at the output terminal are shown in **Fig. 5a-d**, and relevant parameters are summarized in **Table 3**. The dynamic rail-to-rail response of the inverters is in good agreement with the VTC values obtained from **Fig. 4b**. By extracting the rise and fall times of the output waveforms, we are able to determine the corresponding maximum frequency (f_{MAX}) at which the inverters could switch, according to **Equation 2**:

$$f_{MAX} = \frac{2}{t_{PLH} + t_{PHL}} \qquad (2)$$

Here t_{PLH} and t_{PHL} are the propagation delays required for the output waveform to reach the switching threshold for each V_{DD} value in **Fig. 5a-d** from a low state to a high state and vice versa, respectively. As expected, the fastest operation occurs when the inverters are driven at the highest employed V_{DD} (2.0 V), leading to f_{MAX} values of over 100 kHz (**Fig. 5e**). The inverter speed (f_{MAX}) has an exponential dependence on V_{DD}, as evident from the linearity of the corresponding traces plotted in semi-logarithmic scale in **Fig. 5e**. This exponential dependence of the frequency is expected, as the magnitude of the transient current going through one such inverter is exponentially dependent on the V_{DD} employed. Consequently, a higher V_{DD} allows the capacitive load (intrinsic and parasitic) to get charged exponentially faster.

It is noteworthy that the current TFT and inverter layout as well as processing are not optimized for speed. In fact, the current inverter architecture features an overlap between the gate electrode and the semiconductor layer as well as the source and drain electrodes far greater than the channel area ($W_{CH} \times L_{CH}$, where W_{CH} and L_{CH} are the channel width and length of the component transistors). In turn, this results in an equivalent capacitive load C_L at the inverter output terminal far greater than that strictly needed to operate these inverters. In other words, the experimentally-derived f_{MAX} does not correspond to the ultimate speed limit of our low-voltage TFTs and inverters.

Accepted Manuscript

For example, the 350×350 μm^2 overlap (as in this work) of the gate electrode with the sc-SWCNTN results in a capacitance of approximately 800 pF. By contrast, the overlap strictly needed to operate these inverters is determined by the channel dimensions (i.e., W_{CH}×L_{CH}=1000×20 μm^2). The corresponding six-fold lower capacitance (C_{ch} =130 pF) would lead to a six-fold higher speed.

In order to account for the observed transient response, in addition to the overlap capacitance, we also need to consider the external capacitive components contributed by our measurement setup. Due to cabling and probes, we have determined that our measurement setup adds at least 350 pF to C_L. This leads to a total estimated C_L of 1150 pF, which is almost an order magnitude higher than the intrinsic channel capacitance C_{ch}. The weight of the parasitic and external components to

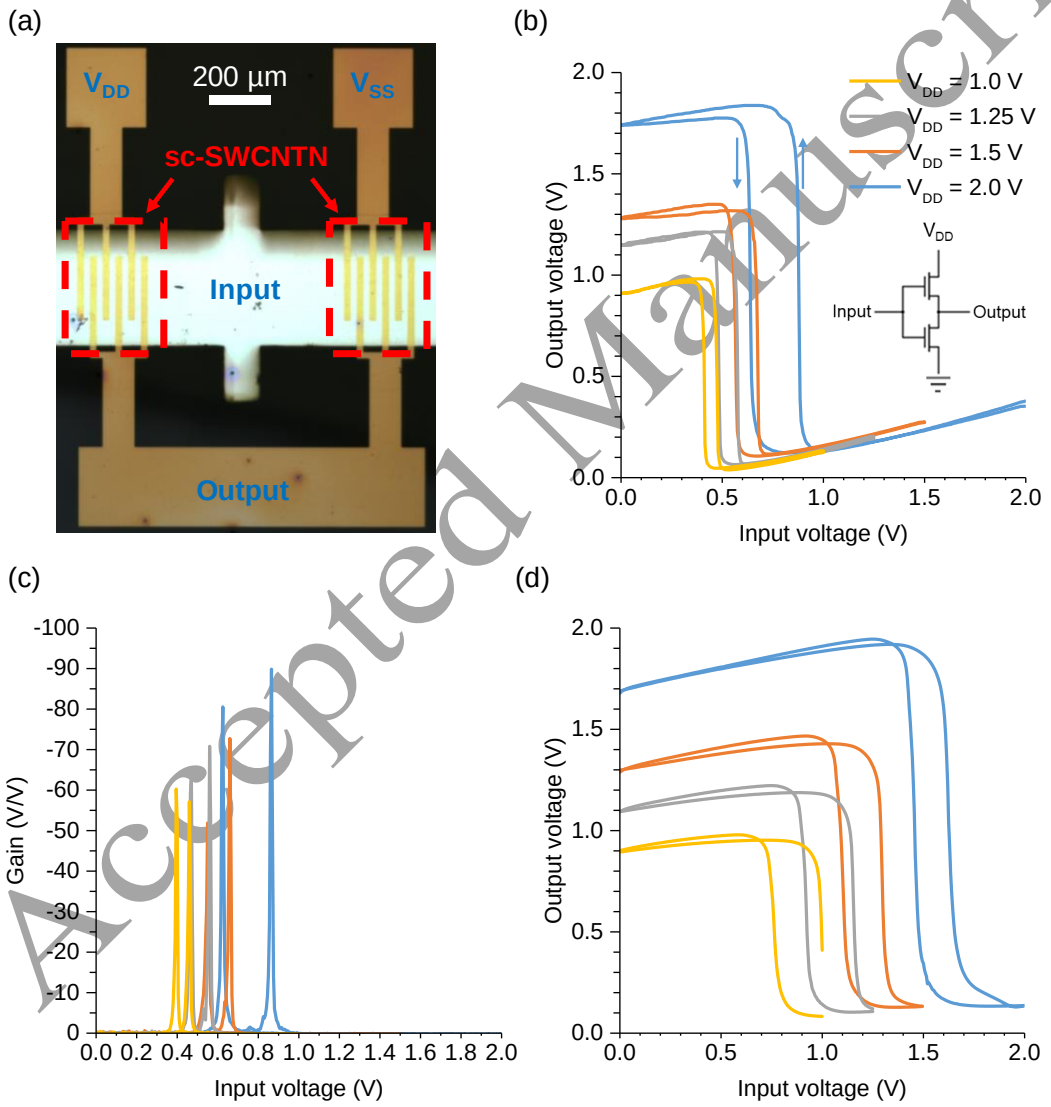

Fig. 4. CMOS-like inverter gates. (a) Micrograph of a fabricated inverter gate. (b) VTCs of an inverter encapsulated with PMMA/CYTOP and operated at different V_{DD} values (inset: schematic of the transistor layout). (c) Gain values derived from the VTCs in (b). (d) VTCs of an inverter relying on non-encapsulated TFTs at different V_{DD} values.

Accepted Manuscript

Table 2
Key parameters of inverters based on PMMA/CYTOP-encapsulated TFTs (extracted from the VTCs in **Fig. 4b**).

V_{DD} (V)	NM_H (%)	NM_L (%)	Gain (V/V)
1.0	0.52	0.43	57
1.25	0.65	0.5	65
1.5	0.7	0.52	70
2.0	1	0.68	86

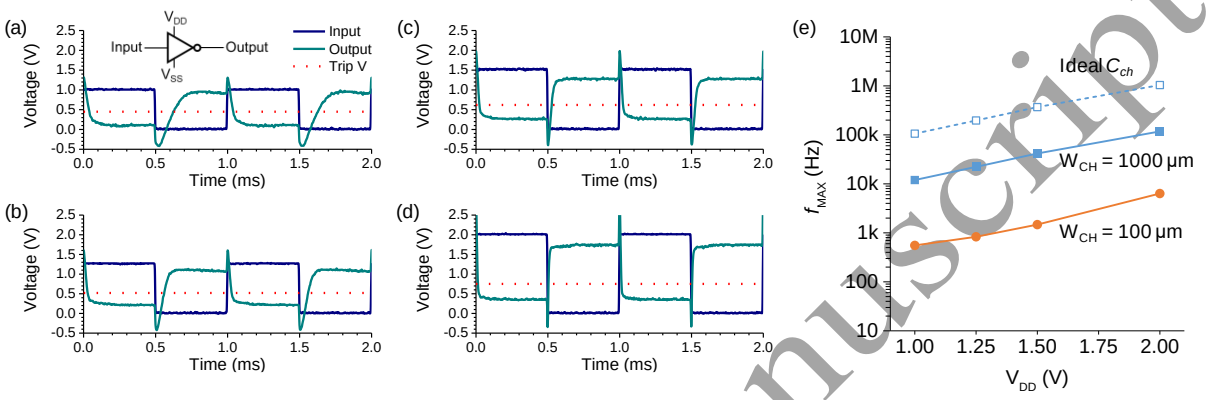

Fig. 5. Transient response of a CMOS-like inverter (with PMMA/CYTOP encapsulation). Output waveforms (blue traces) in response to 1 kHz square waves (teal traces) at the inverter input terminal for (a) V_{DD} = 1.0 V, (b) V_{DD} = 1.25 V, (c) V_{DD} = 1.5 V, and (d) V_{DD} = 2.0 V. The dashed red lines denotes the switching thresholds for each V_{DD}. (e) f_{MAX} vs. V_{DD}, as extracted from the transient response via Equation (2) for inverters with channel width W_{CH} = 1000 µm (data shown in (a)-(d)) as well as for inverters with W_{CH} = 100 µm. The dashed trace in blue corresponds to the limit in which the channel capacitance dominates for W_{CH} = 1000 µm and L_{CH} = 20 µm.

Table 3
Experimental transient response parameters of hybrid-nanodielectric-based inverters with PMMA/CYTOP encapsulation at different V_{DD} values.

V_{DD} (V)	t_{PLH} (µs)	t_{PHL} (µs)	f_{MAX} (kHz)	V_{HIGH} (V)	V_{LOW} (V)
1.0	125	39	12.2	0.95	0.11
1.25	60	28	22.7	1.09	0.23
1.5	27	25	38.5	1.28	0.29
2.0	9	13	112.3	1.74	0.36

C_L is also confirmed by the transient response we measured from an inverter with a channel width W_{CH} ten times smaller (100 µm instead of 1000 µm) than that associated with the response in **Fig. 5a-d**. In such a case, the resulting experimental f_{MAX} is an order of magnitude lower (**Fig. 5e**). The order-of-magnitude reduction of W_{CH} obviously translates in an order-of-magnitude reduction of the charging/discharging current I_t as well as of the channel capacitance C_{ch}. On the other hand, $f_{MAX} \propto I_t/C_L$. Therefore, the order-of-magnitude reduction of f_{MAX} associated with the order-of-magnitude reduction of W_{CH} (**Fig. 5e**) confirms that C_L is dominated by extrinsic (overlap and external) contributions. All things considered, while our circuits already demonstrate a transient response up to the 100 kHz range—e.g., well within the requirements of typical sensing applications—such operating speeds are in fact limited by extrinsic capacitive contributions. Consequently, higher speeds can be achieved in the future by reducing the overlap capacitance

Accepted Manuscript

(e.g., through a self-aligned process; see **Fig. 5e**) as well as by minimizing the impact of the external capacitive load and by decreasing the channel length of the devices below 20 μm.

4. Conclusion

This work has addressed the challenge of achieving low-voltage above-threshold operation with sc-SWCNTN TFTs by boosting the gate-channel coupling through a solution-based approach, thereby overcoming the complexity associated with the ALD deposition of high-κ dielectrics, and the reliability and speed issues associated with ion-gel dielectrics. Specifically, high gate-channel capacitance density was achieved by using an easy-to-fabricate SAM nanodielectric based on a phosphonic-acid molecule. This resulted in sc-SWCNTN TFT devices that could operate in their above-threshold region at low supply voltages (≤ 2 V), while exhibiting well-balanced ambipolar performance with comparable *n*-channel and *p*-channel mobilities (≈ 7 $cm^2 V^{-1} s^{-1}$). Importantly, the devices operated reliably at voltages up to 2 V, proving the robustness of the SAM nanodielectric within such sc-SWCNTN device configuration. In addition to the SAM nanodielectric, key to obtaining these balanced characteristics was the optimization of a thin-film encapsulant based on a spin-on polymer layer. This featured an outer layer made of a highly hydrophobic polymer for greater resilience to environmental factors, in combination with a polymer layer at the interface with the sc-SWCNTN that could preserve the electronic properties of the latter.

The balanced ambipolar characteristics of our sc-SWCNTN TFTs allowed us to fabricate inverter gates in a CMOS-like configuration that could operate at low voltages with positive noise margins. Such inverters delivered switching speeds exceeding 100 kHz at a V_{DD} of 2 V, which is more than suitable for many off-the-grid applications that may require comparatively high speeds (e.g. high sampling rates and/or faster reaction times) in health monitoring and remote sensing for infrastructure monitoring. Furthermore, the analysis of transient measurements in relation to transistor layout revealed that additional improvement in the switching frequency could be achieved in the future by reducing the overlap capacitance without major modifications of the simple fabrication process presented in this work.

Overall, the use of a printed semiconducting active layer consisting of a sc-SWCNTN, an easy-to-fabricate AlO_x/SAM nanodielectric and a spin-on thin-film polymer encapsulation have been integrated successfully, leading to low-voltage above-threshold ambipolar TFTs and digital CMOS-like electronics with state-of-the-art performance, but without the complexity of ALD and the speed and reliability limitations of ion-gel dielectrics. Consequently, the combination of materials, processing, and TFT characteristics presented in this work offers an attractive platform for easy-to-fabricate TFT electronics that can address emerging off-the-grid wearable/sensing applications.

Accepted Manuscript

Conflicts of interest

The authors declare no conflicts of interest.

Credit author contribution statement:

Luis Portilla: Conceptualization, Validation, Formal analysis, Investigation, Writing - Original Draft, Visualization, Funding acquisition.

Jianwen Zhao: Conceptualization, Writing – Review & Editing, Supervision, Funding acquisition.

Jing Zhao: Investigation.

Luigi G.Occhipinti: Writing - Review & Editing.

Vincenzo Pecunia: Conceptualization, Formal analysis, Writing - Original Draft, Supervision, Writing – Review & Editing, Funding acquisition, Project administration.

Data availability

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Acknowledgements:

Funding: The authors acknowledge financial support from the National Natural Science Foundation of China (61950410619, 61950410759, 61805166, 61750110517 and 61874132), the Jiangsu Province Natural Science Foundation (BK20170345), and National Key Research and Development Program of China (2016YFB0401100). Additionally, this work is supported by the Collaborative Innovation Center of Suzhou Nano Science & Technology, the Priority Academic Program Development of Jiangsu Higher Education Institutions (PAPD), the 111 Project, and the Joint International Research Laboratory of Carbon-Based Functional Materials and Devices.

Accepted Manuscript

References

[1] W. Gao, H. Ota, D. Kiriya, K. Takei, A. Javey, Flexible Electronics toward Wearable Sensing, Acc. Chem. Res. 52 (2019) 523–533. https://doi.org/10.1021/acs.accounts.8b00500.

[2] S.J. Kim, S. Yoon, H.J. Kim, Review of solution-processed oxide thin-film transistors, Jpn. J. Appl. Phys. 53 (2014) 02BA02. https://doi.org/10.7567/JJAP.53.02BA02.

[3] J. Zaumseil, Single-walled carbon nanotube networks for flexible and printed electronics, Semicond. Sci. Technol. 30 (2015) 074001. https://doi.org/10.1088/0268-1242/30/7/074001.

[4] V. Pecunia, M. Fattori, S. Abdinia, H. Sirringhaus, E. Cantatore, Organic and Amorphous-Metal-Oxide Flexible Analogue Electronics, Cambridge University Press, 2018. https://doi.org/10.1017/9781108559034.

[5] J.S. Chang, A.F. Facchetti, R. Reuss, A Circuits and Systems Perspective of Organic/Printed Electronics: Review, Challenges, and Contemporary and Emerging Design Approaches, IEEE J. Emerg. Sel. Top. Circuits Syst. 7 (2017) 7–26. https://doi.org/10.1109/JETCAS.2017.2673863.

[6] F.P. García De Arquer, A. Armin, P. Meredith, E.H. Sargent, Solution-processed semiconductors for next-generation photodetectors, Nat. Rev. Mater. 2 (2017) 16100. https://doi.org/10.1038/natrevmats.2016.100.

[7] V. Pecunia, Efficiency and spectral performance of narrowband organic and perovskite photodetectors: a cross-sectional review, J. Phys. Mater. 2 (2019) 042001. https://doi.org/10.1088/2515-7639/ab336a.

[8] S. Ho, S. Liu, Y. Chen, F. So, Review of recent progress in multilayer solution-processed organic light-emitting diodes, J. Photonics Energy. 5 (2015) 057611. https://doi.org/10.1117/1.JPE.5.057611.

[9] Q. Wang, Y. Xie, F. Soltani-Kordshuli, M. Eslamian, Progress in emerging solution-processed thin film solar cells – Part I: Polymer solar cells, Renew. Sustain. Energy Rev. 56 (2016) 347–361. https://doi.org/10.1016/j.rser.2015.11.063.

[10] P. Prakash, K. Mohana Sundaram, M. Anto Bennet, A review on carbon nanotube field effect transistors (CNTFETs) for ultra-low power applications, Renew. Sustain. Energy Rev. 89 (2018) 194–203. https://doi.org/10.1016/j.rser.2018.03.021.

[11] W.A. Gaviria Rojas, M.C. Hersam, Chirality-Enriched Carbon Nanotubes for Next-Generation Computing, Adv. Mater. (2020) 1905654. https://doi.org/10.1002/adma.201905654.

[12] J.A. Cardenas, J.B. Andrews, S.G. Noyce, A.D. Franklin, Carbon nanotube electronics for IoT sensors, Nano Futur. 4 (2020) 012001. https://doi.org/10.1088/2399-1984/ab5f20.

[13] L. Liu, J. Han, L. Xu, J. Zhou, C. Zhao, S. Ding, H. Shi, M. Xiao, L. Ding, Z. Ma, C. Jin, Z. Zhang, L.M. Peng, Aligned, high-density semiconducting carbon nanotube arrays for high-performance electronics, Science (80-.). 368 (2020) 850–856. https://doi.org/10.1126/science.aba5980.

Accepted Manuscript

[14] W.A. Gaviria Rojas, M.C. Hersam, Chirality-Enriched Carbon Nanotubes for Next-Generation Computing, Adv. Mater. (2020) 1905654. https://doi.org/10.1002/adma.201905654.

[15] M.M. Shulaker, G. Hills, N. Patil, H. Wei, H.Y. Chen, H.S.P. Wong, S. Mitra, Carbon nanotube computer, Nature. 501 (2013) 526–530. https://doi.org/10.1038/nature12502.

[16] G. Hills, C. Lau, A. Wright, S. Fuller, M.D. Bishop, T. Srimani, P. Kanhaiya, R. Ho, A. Amer, Y. Stein, D. Murphy, Arvind, A. Chandrakasan, M.M. Shulaker, Modern microprocessor built from complementary carbon nanotube transistors, Nature. 572 (2019) 595–602. https://doi.org/10.1038/s41586-019-1493-8.

[17] J.G. Delgado-Frias, Z. Zhang, M.A. Turi, Near-threshold CNTFET SRAM cell design with removed metallic CNT tolerance, in: Proc. - IEEE Int. Symp. Circuits Syst., IEEE, 2015: pp. 2928–2931. https://doi.org/10.1109/ISCAS.2015.7169300.

[18] J. Tang, Q. Cao, G. Tulevski, K.A. Jenkins, L. Nela, D.B. Farmer, S.J. Han, Flexible CMOS integrated circuits based on carbon nanotubes with sub-10 ns stage delays, Nat. Electron. 1 (2018) 191–196. https://doi.org/10.1038/s41928-018-0038-8.

[19] J.A. Cardenas, J.B. Andrews, S.G. Noyce, A.D. Franklin, Carbon nanotube electronics for IoT sensors, Nano Futur. 4 (2020) 012001. https://doi.org/10.1088/2399-1984/ab5f20.

[20] J.B. Andrews, J.A. Cardenas, C.J. Lim, S.G. Noyce, J. Mullett, A.D. Franklin, Fully Printed and Flexible Carbon Nanotube Transistors for Pressure Sensing in Automobile Tires, IEEE Sens. J. 18 (2018) 7875–7880. https://doi.org/10.1109/JSEN.2018.2842139.

[21] N. Yang, X. Chen, T. Ren, P. Zhang, D. Yang, Carbon nanotube based biosensors, Sensors Actuators, B Chem. 207 (2015) 690–715. https://doi.org/10.1016/j.snb.2014.10.040.

[22] Z. Zhu, An Overview of Carbon Nanotubes and Graphene for Biosensing Applications, Nano-Micro Lett. 9 (2017) 25. https://doi.org/10.1007/s40820-017-0128-6.

[23] A. Chortos, J. Liu, Z. Bao, Pursuing prosthetic electronic skin, Nat. Mater. 15 (2016) 937–950. https://doi.org/10.1038/nmat4671.

[24] L. Xiang, H. Zhang, G. Dong, D. Zhong, J. Han, X. Liang, Z. Zhang, L.M. Peng, Y. Hu, Low-power carbon nanotube-based integrated circuits that can be transferred to biological surfaces, Nat. Electron. 1 (2018) 237–245. https://doi.org/10.1038/s41928-018-0056-6.

[25] N.K. Elumalai, A. Uddin, Open circuit voltage of organic solar cells: An in-depth review, Energy Environ. Sci. 9 (2016) 391–410. https://doi.org/10.1039/c5ee02871j.

[26] S. Kim, R. Vyas, J. Bito, K. Niotaki, A. Collado, A. Georgiadis, M.M. Tentzeris, Ambient RF energy-harvesting technologies for self-sustainable standalone wireless sensor platforms, Proc. IEEE. 102 (2014) 1649–1666. https://doi.org/10.1109/JPROC.2014.2357031.

[27] L. Deng, Z. Wen, X. Zhao, C. Yuan, G. Luo, J. Mo, High voltage output MEMS vibration energy harvester in d31 mode with PZT thin film, J. Microelectromechanical Syst. 23 (2014) 855–861. https://doi.org/10.1109/JMEMS.2013.2296034.

[28] Z. Tehrani, T. Korochkina, S. Govindarajan, D.J. Thomas, J. O'Mahony, J. Kettle, T.C. Claypole, D.T. Gethin, Ultra-thin flexible screen printed rechargeable polymer battery for

Accepted Manuscript

wearable electronic applications, Org. Electron. 26 (2015) 386–394. https://doi.org/10.1016/j.orgel.2015.08.007.

[29] M. Robin, L. Portilla, M. Wei, T. Gao, J. Zhao, S. Shao, V. Pecunia, Z. Cui, Overcoming Electrochemical Instabilities of Printed Silver Electrodes in All-Printed Ion Gel Gated Carbon Nanotube Thin-Film Transistors, ACS Appl. Mater. Interfaces. 11 (2019) 41531–41543. https://doi.org/10.1021/acsami.9b14916.

[30] M. Wei, M. Robin, L. Portilla, Y. Ren, S. Shao, L. Bai, Y. Cao, V. Pecunia, Z. Cui, J. Zhao, Air-stable N-type printed carbon nanotube thin film transistors for CMOS logic circuits, Carbon N. Y. 163 (2020) 145–153. https://doi.org/10.1016/j.carbon.2020.03.012.

[31] L. Portilla, J. Zhao, W. Yan, L. Sun, F. Li, M. Robin, M. Wei, Z. Cui, L.G. Occhipinti, T.D. Anthopoulos, V. Pecunia, Ambipolar Deep-Subthreshold Printed-Carbon-Nanotube Transistors for Ultralow-Voltage and Ultralow-Power Electronics, ACS Nano. (2020) acsnano.0c06619. https://doi.org/10.1021/acsnano.0c06619.

[32] R.P. Ortiz, A. Facchetti, T.J. Marks, High-k organic, inorganic, and hybrid dielectrics for low-voltage organic field-effect transistors, Chem. Rev. 110 (2010) 205–239. https://doi.org/10.1021/cr9001275.

[33] Y. Yang, L. Ding, J. Han, Z. Zhang, L.M. Peng, High-Performance Complementary Transistors and Medium-Scale Integrated Circuits Based on Carbon Nanotube Thin Films, ACS Nano. 11 (2017) 4124–4132. https://doi.org/10.1021/acsnano.7b00861.

[34] H. Zhang, L. Xiang, Y. Yang, M. Xiao, J. Han, L. Ding, Z. Zhang, Y. Hu, L.M. Peng, High-Performance Carbon Nanotube Complementary Electronics and Integrated Sensor Systems on Ultrathin Plastic Foil, ACS Nano. 12 (2018) 2773–2779. https://doi.org/10.1021/acsnano.7b09145.

[35] S.P. Schießl, F. Gannott, S.H. Etschel, M. Schweiger, S. Grünler, M. Halik, J. Zaumseil, Self-Assembled Monolayer Dielectrics for Low-Voltage Carbon Nanotube Transistors with Controlled Network Density, Adv. Mater. Interfaces. 3 (2016) 1600215. https://doi.org/10.1002/admi.201600215.

[36] W. Xu, Z. Liu, J. Zhao, W. Xu, W. Gu, X. Zhang, L. Qian, Z. Cui, Flexible logic circuits based on top-gate thin film transistors with printed semiconductor carbon nanotubes and top electrodes, Nanoscale. 6 (2014) 14891–14897. https://doi.org/10.1039/C4NR05471G.

[37] H. Xiao, H. Xie, M. Robin, J. Zhao, L. Shao, M. Wei, L. Portilla, V. Pecunia, S. Chen, C. Lee, L. Mo, Z. Cui, Polarity tuning of carbon nanotube transistors by chemical doping for printed flexible complementary metal-oxide semiconductor (CMOS)-like inverters, Carbon N. Y. 147 (2019) 566–573. https://doi.org/10.1016/j.carbon.2019.03.003.

[38] F. Zare Bidoky, C.D. Frisbie, Parasitic Capacitance Effect on Dynamic Performance of Aerosol-Jet-Printed Sub 2 v Poly(3-hexylthiophene) Electrolyte-Gated Transistors, ACS Appl. Mater. Interfaces. 8 (2016) 27012–27017. https://doi.org/10.1021/acsami.6b08396.

[39] J.H. Cho, J. Lee, Y. Xia, B. Kim, Y. He, M.J. Renn, T.P. Lodge, C. Daniel Frisbie, Printable ion-gel gate dielectrics for low-voltage polymer thin-film transistors on plastic, Nat. Mater. 7 (2008) 900–906. https://doi.org/10.1038/nmat2291.

[40] M. Halik, H. Klauk, U. Zschieschang, G. Schmid, C. Dehm, M. Schütz, S. Malsch, F.

Accepted Manuscript

Effenberger, M. Brunnbauer, F. Stellacci, Low-voltage organic transistors with an amorphous molecular gate dielectric, Nature. 431 (2004) 963–966. https://doi.org/10.1038/nature02987.

[41] H. Klauk, U. Zschieschang, J. Pflaum, M. Halik, Ultralow-power organic complementary circuits, Nature. 445 (2007) 745–748. https://doi.org/10.1038/nature05533.

[42] A. Cattani-Scholz, Functional Organophosphonate Interfaces for Nanotechnology: A Review, ACS Appl. Mater. Interfaces. 9 (2017) 25643–25655. https://doi.org/10.1021/acsami.7b04382.

[43] S. Casalini, C.A. Bortolotti, F. Leonardi, F. Biscarini, Self-assembled monolayers in organic electronics, Chem. Soc. Rev. 46 (2017) 40–71. https://doi.org/10.1039/C6CS00509H.

[44] M. Halik, A. Hirsch, The potential of molecular self-assembled monolayers in organic electronic devices, Adv. Mater. 23 (2011) 2689–2695. https://doi.org/10.1002/adma.201100337.

[45] C. Zhou, J. Zhao, J. Ye, M. Tange, X. Zhang, W. Xu, K. Zhang, T. Okazaki, Z. Cui, Printed thin-film transistors and NO2 gas sensors based on sorted semiconducting carbon nanotubes by isoindigo-based copolymer, Carbon N. Y. 108 (2016) 372–380. https://doi.org/10.1016/j.carbon.2016.07.035.

[46] H. Xiao, H. Xie, M. Robin, J. Zhao, L. Shao, M. Wei, L. Portilla, V. Pecunia, S. Chen, C. Lee, L. Mo, Z. Cui, Polarity tuning of carbon nanotube transistors by chemical doping for printed flexible complementary metal-oxide semiconductor (CMOS)-like inverters, Carbon N. Y. 147 (2019) 566–573. https://doi.org/10.1016/j.carbon.2019.03.003.

[47] V. Pecunia, K. Banger, A. Sou, H. Sirringhaus, Solution-based self-aligned hybrid organic/metal-oxide complementary logic with megahertz operation, Org. Electron. 21 (2015) 177–183. https://doi.org/10.1016/j.orgel.2015.03.004.

[48] S.D. Brotherton, Introduction to thin film transistors: Physics and technology of TFTs, Springer International Publishing, Heidelberg, 2013. https://doi.org/10.1007/978-3-319-00002-2.

[49] A. Lekawa-Raus, L. Kurzepa, G. Kozlowski, S.C. Hopkins, M. Wozniak, D. Lukawski, B.A. Glowacki, K.K. Koziol, Influence of atmospheric water vapour on electrical performance of carbon nanotube fibres, Carbon N. Y. 87 (2015) 18–28. https://doi.org/10.1016/j.carbon.2015.02.018.

[50] C.M. Aguirre, P.L. Levesque, M. Paillet, F. Lapointe, B.C. St-Antoine, P. Desjardins, R. Martel, The role of the oxygen/water redox couple in suppressing electron conduction in field-effect transistors, Adv. Mater. 21 (2009) 3087–3091. https://doi.org/10.1002/adma.200900550.

[51] Q. Qian, G. Li, Y. Jin, J. Liu, Y. Zou, K. Jiang, S. Fan, Q. Li, Trap-state-dominated suppression of electron conduction in carbon nanotube thin-film transistors, ACS Nano. 8 (2014) 9597–9605. https://doi.org/10.1021/nn503903y.

[52] F. Lapointe, A. Sapkota, J. Ding, J. Lefebvre, Polymer Encapsulants for Threshold Voltage Control in Carbon Nanotube Transistors, ACS Appl. Mater. Interfaces. 11 (2019) 36027–36034. https://doi.org/10.1021/acsami.9b09857.

Accepted Manuscript

[53] V. Jokinen, P. Suvanto, A.R. Garapaty, J. Lyytinen, J. Koskinen, S. Franssila, Durable superhydrophobicity in embossed CYTOP fluoropolymer micro and nanostructures, Colloids Surfaces A Physicochem. Eng. Asp. 434 (2013) 207–212. https://doi.org/10.1016/j.colsurfa.2013.05.061.

[54] H. Lim, Y. Lee, S. Han, J. Cho, K.-J. Kim, Surface treatment and characterization of PMMA, PHEMA, and PHPMA, J. Vac. Sci. Technol. A Vacuum, Surfaces, Film. 19 (2001) 1490–1496. https://doi.org/10.1116/1.1382650.

[55] J. Chen, X. Xiong, Q. Zhang, L. Shui, S. Shen, H. Yang, Z. Zhu, F. Zhang, P(VDF-TrFE)/PMMA blended films with enhanced electrowetting responses and superior energy storage performance, Polymers (Basel). 11 (2019) 526. https://doi.org/10.3390/polym11030526.

[56] E.J. Meijer, D.M. De Leeuw, S. Setayesh, E. Van Veenendaal, B.H. Huisman, P.W.M. Blom, J.C. Hummelen, U. Scherf, T.M. Klapwijk, Solution-processed ambipolar organic field-effect transistors and inverters, Nat. Mater. 2 (2003) 678–682. https://doi.org/10.1038/nmat978.

[57] J.P. Uyemura, Fundamentals of MOS Digital Integrated Circuits, Addison-Wesley Longman Publishing Co., Inc., 1989. https://doi.org/10.1016/0167-9260(89)90026-6.

Accepted Manuscript

Ambipolar Carbon Nanotube Transistors with Hybrid Nanodielectric for Low-Voltage CMOS-like Electronics

Authors: Luis Portilla[1,2], Jianwen Zhao[2*], Jing Zhao[1], Luigi. G. Occhipinti[3], Vincenzo Pecunia[1*]

Affiliations

[1]Jiangsu Key Laboratory for Carbon-Based Functional Materials & Devices, Institute of Functional Nano & Soft Materials (FUNSOM), Joint International Research Laboratory of Carbon-Based Functional Materials and Devices, Soochow University, 199 Ren'ai Road, Suzhou, 215123 Jiangsu, China.

[2]Printable Electronics Research Centre, Suzhou Institute of Nanotech and Nano-bionics, Chinese Academy of Sciences, No. 398 Ruoshui Road, SEID, Suzhou Industrial Park, Suzhou, Jiangsu Province, 215123, China.

[3]Department of Engineering, University of Cambridge, 9 JJ Thomson Avenue, Cambridge CB3 0FA, United Kingdom.

*Correspondence to: jwzhao2011@sinano.ac.cn (Jianwen Zhao); vp293@suda.edu.cn (Vincenzo Pecunia).

Accepted Manuscript

SI1. Surface characterization via XPS

The thickness of the plasma generated AlO_x layer was estimated via X-ray Photoelectron Spectroscopy (XPS) according to the method proposed by B. R. Strohmeier, which is based on the relative magnitudes of the Al peak vs. Al-oxide peak [1]. Specifically, the thickness (d) was extracted using the following formula:

$$d = 28 \ln\left(\left(1.4\left(\frac{I_o}{I_m}\right)\right) + 1\right)$$

where I_m and I_o are the areas of the metal and oxide peaks respectively. Using the values extracted from the XPS measurement (**Fig. S1a**), we have obtained an AlO_x thickness of 3.4 nm, which is in very good agreement with the literature values from AlO_x dielectrics fabricated through the same procedure [2,3]. Furthermore, a qualitative confirmation of the C_{18}-PA SAM atop the plasma generated AlO_x can also be confirmed via the measurements presented in **Fig. S1a-b**. This can be inferred from the reduction of intensity of the Al-metal and Al-oxide peaks (**Fig. S1a**) that is present when the same measurement is conducted between the pure AlO_x layer and the C_{18}-PA SAM covered AlO_x. The decrease of the peak intensity is caused by the attenuation of the XPS signal which originates from the presence of the C_{18}-PA SAM atop the AlO_x layer [4]. Additional corroboration of the existence of the C_{18}-PA SAM layer is obtained via the carbon (C1s) region. Specifically, the C-C peaks presented in **Fig. S1b** show an increased peak intensity for the sample with the C_{18}-PA SAM, as would be expected from the 18-carbon-long alkyl chain of the C_{18}-PA SAM. Finally, the C-C peak present in the plasma AlO_x sample is attributed to adventitious carbon contamination due to exposure of the sample to the environment.

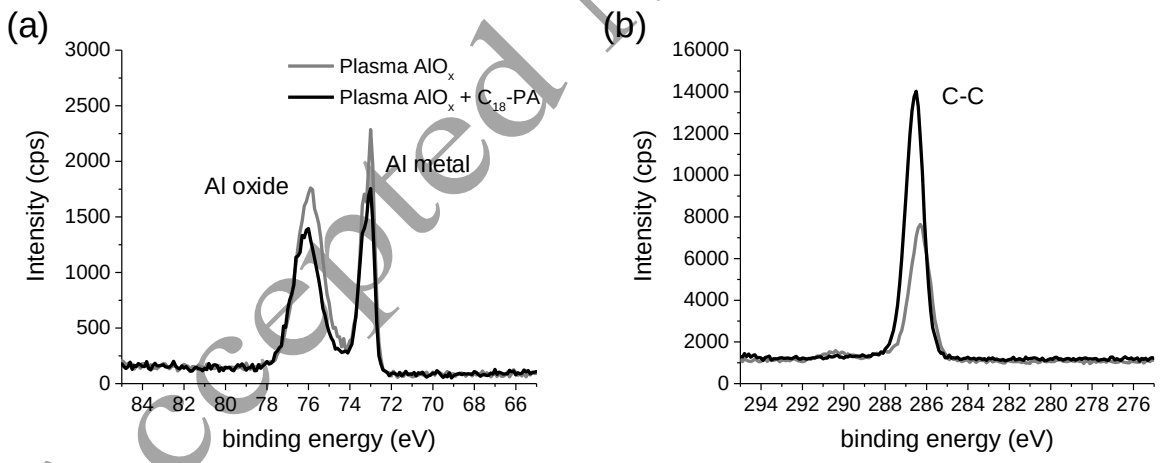

Fig. S1. Relevant XPS scans of a plasma generated AlO_x surface with and without the C_{18}-PA SAM. (a) Al and Al-oxide (Al2p) region. (b) Carbon (C1s) region.

Accepted Manuscript

SI2. C_{18}-PA SAM coverage

We have estimated the SAM surface coverage of our nanodielectric using an impedance-based approach [5–7]. Let us indicate with $C_{SAM|OX}$ the areal capacitance obtained when the SAM covers the AlO_x layer with a surface coverage of 100%. Considering the series combination of the capacitance associated with the SAM (areal capacitance: C_{SAM}) and the capacitance associated with the oxide (areal capacitance: C_{OX}), $C_{SAM|OX}$ reads:

$$C_{SAM|OX} = \frac{C_{SAM} C_{OX}}{C_{SAM} + C_{OX}}$$

Furthermore, in a nanodielectric in which the SAM does not fully cover the oxide layer, the overall areal capacitance is equivalent to the parallel combination of: a) the capacitance associated with the regions that are not covered by the SAM (areal capacitance: C_{OX}); and b) the capacitance associated with the regions that are covered by the SAM (areal capacitance: $C_{SAM|OX}$). These two components contribute to the total equivalent capacitance in accordance with the fractional surface coverage c of the SAM, giving a total areal capacitance C_{TOT} that amounts to:

$$C_{TOT} = c \cdot C_{SAM|OX} + (1 - c) \cdot C_{OX}$$

Our electrical characterization of the SAM-based and oxide-only nanodielectrics gives direct access to both C_{OX} of 1.74 μF/cm^2 and C_{TOT} of 0.65 μF/cm^2 for C_{18}-PA-SAM/AlO_x. Additionally, $C_{SAM} = \varepsilon_0 \varepsilon_{SAM} / t_{SAM}$, where ε_0 is the permittivity of vacuum, ε_{SAM} is the dielectric constant of the SAM molecule and t_{SAM} is the thickness of the SAM layer. The values ε_{SAM} = 2.5 and t_{SAM} = 2.3 nm for the C_{18}-PA SAM are well-documented in the literature [3,8,9]. Based on all of the above, we obtain that the surface coverage of the C_{18}-PA SAM that amounts to 98%. These values are fully consistent with the literature—within the instrumental error—and confirm the full surface coverage of the SAMs in our nanodielectric.

Accepted Manuscript

SI3. Transfer curves for parameter extraction

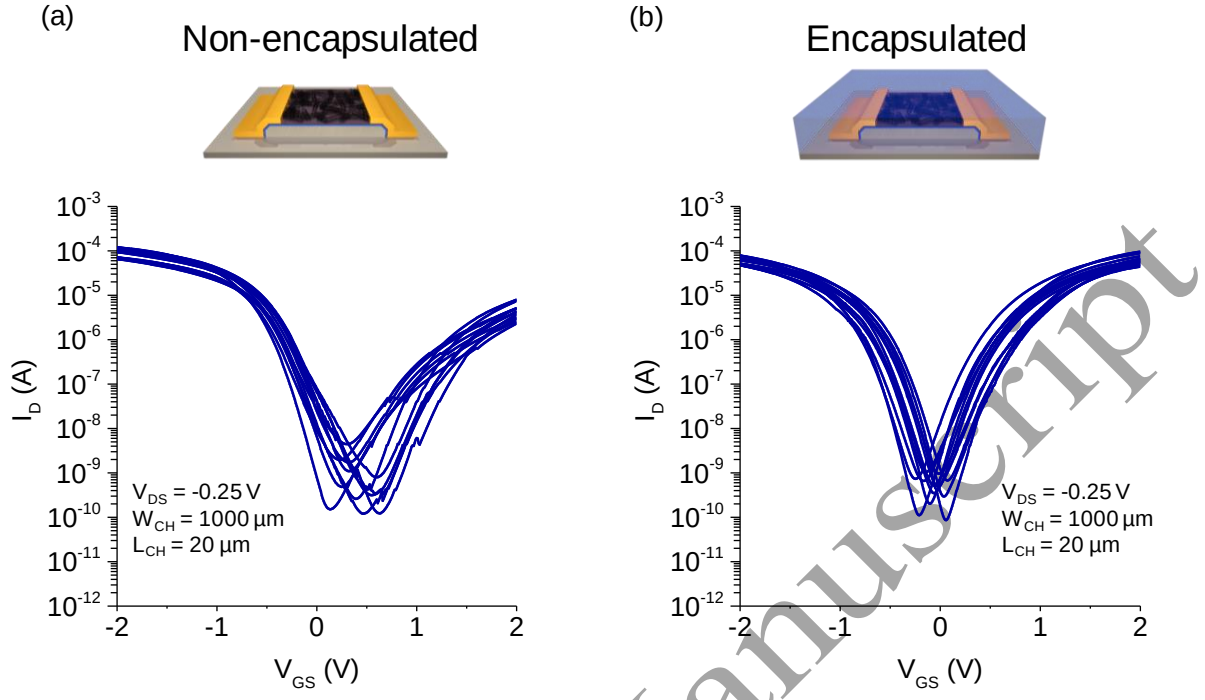

Fig. S3. Mobility. (a) Transfer curves employed for the parameter extraction of non-encapsulated devices. (b) Transfer curves employed for the mobility extraction of PMMA/CYTOPS encapsulated devices.

The linear mobility was extracted with the equation for the linear mobility of field effect transistors, $\mu_{lin} = (L_{CH}/W_{CH}C_{ox}V_{DS}) \cdot (\partial I_D/\partial V_{GS})$ in here W_{CH} corresponds to the channel width and L_{CH} to the channel length, C_{ox} is the areal capacitance of the dielectric employed, V_{DS} is the drain-source voltage, I_D is the drain current and the gate voltage V_{GS}. The value of C_{ox} is extracted from Fig 1c.

Accepted Manuscript

SI4. Formula for calculating trap density

Calculated trap densities as per Eq. S1 for encapsulated and non-encapsulated devices.

$$D_{tr} = \frac{C_{OX}}{q}\left(SS\frac{\log(e)}{kT/q} - 1\right) \quad \text{(S1)}$$

Here C_{OX} is the capacitance density of the dielectric, q is the elementary charge, SS is the average subthreshold swing, k is the Boltzmann's constant, and T is the absolute temperature.

SI5. Noise margin of inverters

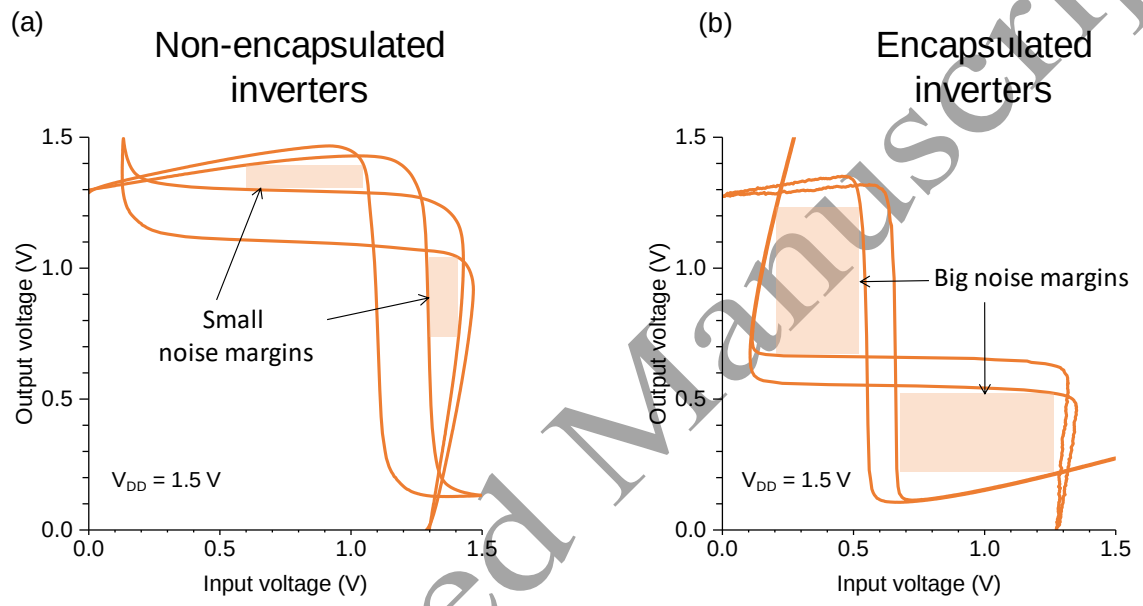

Fig. S5. Noise margins. (a) Noise margins of non-encapsulated inverters. (b) Noise margins encapsulated inverters.

Accepted Manuscript

References

[1] B.R. Strohmeier, An ESCA method for determining the oxide thickness on aluminum alloys, Surf. Interface Anal. 15 (1990) 51–56. https://doi.org/10.1002/sia.740150109.

[2] H. Klauk, U. Zschieschang, J. Pflaum, M. Halik, Ultralow-power organic complementary circuits, Nature. 445 (2007) 745–748. https://doi.org/10.1038/nature05533.

[3] A. Khassanov, H.-G. Steinrück, T. Schmaltz, A. Magerl, M. Halik, Structural Investigations of Self-Assembled Monolayers for Organic Electronics: Results from X-ray Reflectivity, Acc. Chem. Res. 48 (2015) 1901–1908. https://doi.org/10.1021/acs.accounts.5b00022.

[4] C.L.A. Lamont, J. Wilkes, Attenuation Length of Electrons in Self-Assembled Monolayers of n -Alkanethiols on Gold, Langmuir. 15 (1999) 2037–2042. https://doi.org/10.1021/la981168p.

[5] S. Campuzano, M. Pedrero, C. Montemayor, E. Fatás, J.M. Pingarrón, Characterization of alkanethiol-self-assembled monolayers-modified gold electrodes by electrochemical impedance spectroscopy, J. Electroanal. Chem. 586 (2006) 112–121.

https://doi.org/10.1016/j.jelechem.2005.09.007.
[6] P. Diao, M. Guo, R. Tong, Characterization of defects in the formation process of self-assembled thiol monolayers by electrochemical impedance spectroscopy, J. Electroanal. Chem. 495 (2001) 98–105. https://doi.org/10.1016/S0022-0728(00)00424-1.
[7] R.V. Jagadeesh, V. Lakshminarayanan, Adsorption kinetics of phosphonic acids and proteins on functionalized Indium tin oxide surfaces using electrochemical impedance spectroscopy, Electrochim. Acta. 197 (2016) 1–9. https://doi.org/10.1016/j.electacta.2016.03.008.
[8] A. Jedaa, M. Burkhardt, U. Zschieschang, H. Klauk, D. Habich, G. Schmid, M. Halik, The impact of self-assembled monolayer thickness in hybrid gate dielectrics for organic thin-film transistors, Org. Electron. 10 (2009) 1442–1447. https://doi.org/10.1016/j.orgel.2009.08.006.
[9] R. Luschtinetz, A.F. Oliveira, H.A. Duarte, G. Seifert, Self-assembled Monolayers of Alkylphosphonic Acids on Aluminum Oxide Surfaces - A Theoretical Study, Zeitschrift Für Anorg. Und Allg. Chemie. 636 (2010) 1506–1512. https://doi.org/10.1002/zaac.201000016.

Accepted Manuscript