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High-Performance Solution-Processed Amorphous-Oxide-Semiconductor TFTs with Organic Polymeric Gate Dielectrics

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Abstract. In this study we investigate the behavior of solution-processed metal-oxide-semiconductor transistors utilizing organic polymeric gate dielectrics. By adopting organic dielectrics covering a range of chemistries and relative permittivity values, we demonstrate the general outstanding performance of the resulting hybrid devices, which feature state-of-the-art charge-carrier mobility and the capability of low voltage operation, while allowing solution-based processing. Furthermore, we show the extraordinary stability of these transistors under constant-current bias stress.

Keywords: amorphous metal-oxide semiconductors, organic dielectrics, hybrid thin-film transistors, solution-processed transistors, bias-stress stability

Solution-processed amorphous metal-oxide semiconductors (AMOxSs) have the potential to play a primary role in the development of large-area electronics, given their outstanding charge-carrier mobility and ease of processing.[1–3] Thin-film transistors (TFTs) based on such semiconductors, however, are yet to achieve full solution processability for their potential to be actualized. In fact, the metal-oxide-semiconductor community has thus far primarily focused on inorganic dielectrics, such as SiN_x,[4] AlO_x,[5,6] ZrOx,[7] HfO_x,[8,9] and TaO_x,[10] on the basis of their atomic interface structures and thermo-mechanical properties being similar to the ones of AMOxSs. In most cases these dielectrics are deposited in vacuum (by RF-magnetron sputtering,[11,12] ALD,[13] and PECVD.[4,14] Their solution-based deposition has also been demonstrated, with process temperatures typically in the region of 300 ºC,[6,9,15–18] or at dramatically lower values if in combination with UV exposure.[19] Other gate-dielectric routes that have been explored include self-assembled nanodielectrics and polyelectrolytes.[20–

[23] Finally, few isolated reports deal with amorphous metal-oxide transistors with a polymeric gate dielectric (predominantly cross-linked PVP).[24,25]

A pressing concern within the AMOxS community is low-voltage TFT operation, which demands a strong capacitive coupling between the gate electrode and the semiconductor. A commonly explored route consisted in using high-κ inorganic materials (i.e., SiN_x, AlO_x, ZrO_x, HfO_x). It was found challenging, however, to achieve stable transistor operation and low gate leakage currents with gate dielectrics of this class,[10,26–28] in view of the large band gap of AMOxSs (> 3 eV) and the observed inverse correlation in inorganic dielectrics between relative permittivity and bandgap.[29,30] In fact, minimum energy offsets (≈ 1 eV) between the conduction/valence bands of the semiconductor and the gate dielectric are needed to confine the charge carriers at the active interface and minimize undesirable charge injection from the semiconductor into the gate dielectric.[31]

Given the great interest in achieving full solution processability of metal-oxide-based transistors, here we present a comprehensive study on the general applicability of organic polymeric insulators as their gate dielectrics, and investigate the dependence of device performance on the polymer dielectric constant. We discuss the expected energy-level alignment with amorphous metal-oxide semiconductors, and present a detailed analysis of the field-effect mobilities, subthreshold slopes, interfacial trap densities, and gate leakage of the AMOxS transistors. We demonstrate in particular that high-κ polymeric gate dielectrics exhibit excellent performance in combination with AMOxSs and allow low-voltage TFT operation below 5 V. Finally, we illustrate the outstanding electrical stability of our devices under constant-current stress, which highlights the strength of the polymeric route to fully solution-processable AMOxS transistors.

Experimental Section

All our TFTs were produced in the staggered top-gate geometry on Corning® 1737 slides. The source and drain electrodes, consisting of thermally-evaporated gold (20 nm thick) on an ultra-thin chromium adhesion layer (1 nm thick), were patterned by conventional photolithography into an interdigitated structure having a channel length of L = 10 μm and a channel width of W = 1 mm. After source and drain deposition and patterning, we coated our samples with the metal-oxide precursor, which was subjected to the annealing step detailed in the following. The resulting metal-oxide film was then patterned via conventional wet etching in diluted hydrochloric acid,[32] so to confine it to the regions around the source and drain electrodes. Subsequently, we coated the samples with an organic polymeric dielectric spun from a solution in a suitable organic solvent. Finally, aluminum gate electrodes (40nm thick) were thermally evaporated through a shadow mask directly above the transistor active regions. The solution-based amorphous metal-oxide semiconductor utilized in this work is an indium-zinc oxide (IZO, with an 8:2 blending ratio of the alkoxide-based indium and zinc precursors) produced in thin-film form according to the 'sol–gel on chip' method described elsewhere.[3,33] Banger et al. demonstrated transistor operation of this specific IZO in bottom-gate staggered TFTs having SiO_2 and Al_2O_3 as gate dielectric, with a reported electron mobility monotonically dependent on annealing temperature.[33] The two-hour-long annealing treatment we subjected our metal-oxide films to was carried out in air at 275 ºC and under UV illumination (at a wavelength of 254 nm and with a 5−8 mW cm^{-2} irradiance).

Our TFTs comprise organic polymeric dielectrics whose repeat units are shown in **Table 1**: CYTOP™, an amorphous fluoropolymer of the PTFE family; poly(α-methylstyrene) (PαMS), a hydrophobic polymer with a phenyl functionality; poly(styrene-co-acrylonitrile) (SAN), a copolymer with nitrile functionality; poly(bisphenol A carbonate) (PC), a stiff thermoplastic with outstanding thermal stability; poly(methyl methacrylate) (PMMA), a ubiquitous polyacrylate with excellent optical transparency; P(VDF-TrFE-CFE), a fluorinated relaxor

ferroelectric terpolymer, referred to as FRFT in the following. CYTOP™ was purchased from Asahi Glass Co. Ltd., PαMS from Polymer Source Inc., SAN and PC from Scientific Polymer Inc., PMMA from Sigma-Aldrich®, and the FRFT from Piezotech SAS. Except CYTOP™, which was received in solution, all the other polymers came in the form of pellets or powder and were dissolved in suitable anhydrous organic solvents: PαMS was dissolved in xylene at a concentration of 60 mg mL^{-1}; SAN in butyronitrile at 40 mg mL^{-1}; PC in 1,2-dichlorobenzene at 80 mg mL^{-1}; PMMA in n-butyl acetate at 40 mg mL^{-1}; FRFT in n-butyl acetate at 40 mg mL^{-1}. The polymers were all deposited by spin coating at angular speeds in the region of 2000−5000 rpm. The spin coating was carried out in a nitrogen glovebox with ppm levels of both oxygen and water. Their resulting thickness is in the region of 100−200 nm, except for the CYTOP™ films, for which t_I = 330nm. Their thermal curing (i.e., drying) was conducted at 80 ºC.

The current-voltage characterization of our transistors was performed at room temperature in a nitrogen-atmosphere glovebox (with oxygen concentration below 2 ppm at all times) utilizing an HP4155C SPA (Agilent Technologies). The reported transistor mobility was calculated from the linear transfer characteristics as $\mu = (V_{DS}\, C_I\, W/L)^{-1}\, (dI_{DS}/dV_{GS})$, where C_I is the gate dielectric capacitance per unit area.

Impedance analysis was used to characterize the relative permittivity of our polymeric dielectrics, from which we derived the field-effect capacitance of our TFTs. Metal-insulator-metal (MIM) structures were produced to this end, the impedance of which was measured with an HP4192A impedance analyzer (Agilent Technologies). MIM structures with different areas were utilized (the MIM structures had round electrodes with radius equal to 250 μm, 500 μm, and 1000 μm), so that the slope of the linear interpolant of the capacitance-area dataset would give the parasitic-free capacitance per unit area. The latter value was then multiplied by the film thickness to determine the dielectric permittivity.

Ultraviolet-visible absorbance of our organic thin films was measured in air through an HP845x spectrometer. The films of interest were deposited on Spectrosil® 2000 substrates, given their extremely low cut-off wavelength of about 200 nm. Bare substrates were used as the baseline for all spectra.

Results and Discussion

Dielectric Characterization. As a preliminary evaluation of the suitability of the selected polymeric insulators as gate dielectrics for AMOxS TFTs, we assessed their energy gaps by means of UV-vis transmission spectrometry. In fact, for an insulator to allow the charge confinement required for transistor performance, it is crucial that its energy band offsets with respect to the semiconductor are sufficiently large, and greater than approximately 1 eV.[31] Were this not the case, charge would be injected into the dielectric at small or moderate electric fields, causing a reduction in accumulated charge at the interface, an increase in gate current, and a deterioration of device stability. While this requirement is easily met by a great number of polymeric insulators with respect to a variety of semiconductors (e.g., organic semiconductors), the very large bandgap of AMOxSs (e.g., 3 eV for our IZO) makes it considerably more restrictive. Indeed, for charge confinement to be achieved in combination with an AMOxS, the gate dielectric should have a bandgap of at least 5 eV, with this lower limit corresponding to the best-case scenario in which the frontier energy bands of the dielectric are symmetrically located around the ones of the semiconductor.

The optical gaps of the selected polymers, extracted from their UV-vis absorbance (see Supporting Information), are indicated in Table 1. Both our fluorinated polymers do not show appreciable absorption in the measured range, thus suggesting an optical gap greater than 6 eV, well above the charge confinement limit for AMOxSs. All our non-fluorinated polymers, instead, exhibit an optical gap in the region of 5 eV, at the limit for charge confinement for AMOxSs.

To fully exploit the high charge-carrier mobility that AMOxSs are capable of, it is imperative that the gate dielectric has a consistent polarization up to frequencies in the megahertz region. The dielectric response of the selected polymers was characterized with an impedance analyzer, using thin-film MIM structures (polymer film thickness ≈ 200 nm). The extracted relative permittivities are listed in Table 1. The dielectric response is constant within the instrumental frequency range (up to 1 MHz) for all the low-κ materials, making them ideal candidates for stable and high-speed AMOxS-based TFTs (given the absence of slow polarization effects). The very large permittivity of our FRFT, instead, manifests a pronounced relaxation at frequencies higher than 40 kHz, and an appreciable field dependence beyond 400 kV cm^{-1} (see Supporting Information), thus confirming the behavior reported for terpolymers of the same class.[34,35] As a consequence, this latter polymeric dielectric would lend itself to low-voltage transistor operation, but bearing a significant limitation in operational speed and driving gate voltage.

Transistor Characteristics and Performance Parameters. Given the preliminary assessment above, all our selected polymeric insulators are potential candidates as gate dielectrics in AMOxS-based TFTs. To explore this possibility, we fabricated top-gate staggered TFTs with each of the polymeric dielectrics in combination with our IZO. In **Figure 1a** we show representative transfer characteristics of the resulting TFTs, acquired for a symmetric double gate voltage sweep applied in continuous mode. The TFTs were all operated in the linear region with V_{DS} = 1 V. Hysteresis-free transistor behavior was observed for all the tested devices, with on/off ratios at the same level (10^8) as those reported for IZO devices utilizing SiO_2 as gate dielectric.[33] The maximum gate voltage applied to all TFTs was such that the devices were subjected to a maximum gate field in the region of 4 MV cm^{-1}, with the only exception being the FRFT TFTs, for which much lower gate fields were applied to achieve equivalent current levels. In all samples the gate current in electron accumulation was close to the detection limit of our instrumentation, denoting a gate leakage below 10 nA cm^{-2}, the

latter value being reached at the maximum applied field. For negative gate voltages the situation was the same, except for the PαMS and PC TFTs, which were characterized by a slight increase in gate current (also reflected in the source and drain current) beyond an electric field greater than about 2 MV cm^{-1}. The extremely low gate leakage for both voltage polarities suggests that these polymeric dielectrics are capable of providing the energy barrier necessary for charge confinement. Following Robertson's argument,[31] we speculate that these dielectrics allow energy-band offsets in the region of or greater than 1 eV.

We also measured the output characteristics of all our TFTs, a sample of which is shown in **Figure 1b**. They exhibit a linear behavior close to the origin of the I_{DS}-V_{DS} plane, indicating low contact resistance. As expected, the TFTs with the FRFT gate dielectric achieve low-voltage transistor operation (within a voltage range of the order of 1 V), showing the versatility of this class of terpolymers in combination with inorganic semiconductors.[36]

We extracted the linear field effect mobility of a number of TFTs comprising each of the selected polymeric dielectrics in combination with IZO. Given the differences in permittivity and thickness, it is best to express the mobility as a function of charge density for a fair comparison of the performance of all these transistors, as shown in **Figure 2a**. Specifically, following the approximation proposed by Hoffman,[37] we estimated the induced charge density as $Q_{ind} = C_I (V_{GS} - V_{ON})$, where V_{ON}, the transistor onset voltage, was taken as the V_{GS} at which I_{DS} = 100 pA (for V_{DS} = 1V). Figure 2a shows that the mobility varies roughly linearly with Q_{ind}, although a saturation effect may occur at high charge densities, as suggested by the change in slope of the PMMA trace. Mobility values in the range of 2−6 $cm^2 V^{-1} s^{-1}$ are extracted from all our TFTs, comparable with the ones obtained for the same semiconductor in bottom-gate devices with thermal SiO_2 as gate dielectric.[33]

The dataset in Figure 2a does not allow us to resolve the minor differences in mobility between samples having gate dielectrics with similar permittivities, particularly the ones with PMMA, SAN, and PC. Over a larger range of permittivities, however, a trend is apparent, as

the CYTOP™ TFTs (with $\kappa = 2.1$) give a significantly higher mobility than the ones using FRFT ($\kappa = 40$), while the samples with intermediate permittivities result in intermediate mobility values. The dependence of the mobility on the permittivity, however, is rather weak compared to what was observed for organic semiconductors, the other major class of semiconductors in the same mobility range as AMOxSs. In fact, for both semiconducting polymers[38,39] and organic crystalline molecular films,[40,41] the mobility changes by orders of magnitude with the relative permittivity of the gate dielectric. In this latter class of materials the effect was found to derive from the coupling between the charge carriers and the polar environment dictated by the gate dielectric, which is strong given the very high effective mass of the charge carriers in organic semiconductors. The weak dependence of the mobility on relative permittivity we observe in our hybrid AMOxS-based TFTs suggests that such interaction is much weaker for electrons in IZO, as it can be expected from their very low effective mass.[42,43]

The subthreshold slope extracted from the linear transfer characteristics of our hybrid TFTs manifests an inverse dependence on the relative permittivity of the gate dielectric, with the CYTOP™ TFTs giving the highest values (≈ 2 V dec^{-1}) and the FRFT TFTs the lowest (≤ 100 mV dec^{-1}, nearly an order of magnitude lower than the other TFTs, and quite close to the theoretical limit at room temperature[44]). We used these values to estimate the effective trap state density N_{eff} at the semiconductor-dielectric interface through the equation $S = k\,T / q\,\log(10)\,(1 + q^2 / C_I\,N_{eff})$.[44] The estimated densities are shown in **Figure 2b**. They are in the region of 10^{12} cm^{-2} eV^{-1}, except for the FRFT TFTs, which yield significantly lower values. From this we gather that the decreasing trend observed in the subthreshold slope is primarily determined by the stronger gate-to-channel capacitive coupling allowed by gate dielectrics with higher permittivity. In this respect, the much lower subthreshold slope and reduced trap state density show the potential of FRFT as the gate dielectric for low-voltage hybrid TFTs.

The extracted trap state densities are perfectly aligned with the literature values for bottom-gate TFTs with sputtered and solution-processed AMOxSs and employing inorganic gate dielectrics.[45–48] When compared with the top-gate AMOxS TFTs reported in the literature, a distinction must be made on the basis of the deposition technique employed for the gate dielectric. Indeed, our hybrid TFTs show trap state densities matching the values of top-gate devices with gate dielectrics deposited by ALD and PECVD,[49] but are superior to the ones fabricated with sputtered dielectrics.[50]

Constant-Current Bias Stress. Constant-current transistor operation is of great technological importance, as it directly relates to the possibility of using the TFTs in one of the most attractive applications of all, namely AMOLED displays. Specifically, it has been estimated that TFTs are to be capable of supplying a current of 250 nA for an equivalent aspect ratio of $W / L = 5$ to meet the required performance level.[51]

Constant-current bias-stress experiments were performed on our TFTs comprising all the selected polymeric dielectrics. In these stress experiments, the TFTs were subjected to a constant current of 5 μA so to conform to the operational requirement mentioned above. Gate and drain electrodes were shorted throughout the duration of the stress, which was interrupted only for the measurement of the transistor transfer characteristics at logarithmically spaced times.

Figure 3 shows the shift in gate voltage necessary to maintain the constant current over a stress time of 14 h. The spikes present in each trace are due to the transient charging of the channel after measuring the transfer characteristics. Two kinds of behavior emerge: on one hand, the TFTs with the FRFT dielectric undergo a negative gate voltage shift; on the other, the rest of the TFTs exhibit a positive gate-voltage shift. The overall shifts are extremely small, especially considering the sizeable stress time: in the TFTs with low-κ dielectrics $\Delta V_G \leq 0.7$ V, and in the PC, SAN and PMMA ones the shift is as low as 0.1 V; the FRFT sample, instead, gives $\Delta V_G = -0.5$ V.

In the TFTs with low-κ dielectrics, the differences in bias-stress behavior are likely to arise from sample-to-sample variations, given that the traces are very close to one another. All of them give a matching shift of onset and threshold voltages, along with a constant subthreshold slope (see Supporting Information). Moreover, mobility as a function of gate voltage is rigidly shifted in the direction of the applied bias. As for the terpolymer device, its bias-stress behavior takes the form of a progressive degradation of the subthreshold slope and an increase of the on current (see Supporting Information). All these findings suggest that charge trapping is the cause of the observed degradation for the TFTs with low-κ dielectrics, whereas a slow polarization effect may yield the FRFT device behavior. We fitted the threshold voltage shift of the low-κ devices with the conventional power law for constant-current bias-stress,[52] but the extracted fitting parameters are characterized by a large uncertainty due to their small gate voltage shifts. Finally, we note that the observed stability of our hybrid solution-based TFTs is on par with the one reported under equivalent stress conditions for state-of-the-art oxide devices produced by vacuum techniques.[53]

Conclusions

In this study we demonstrated the wide applicability of organic polymeric insulators as gate dielectrics in metal-oxide-semiconductor transistors, which give state-of-the-art mobility, on-off current ratios, and trap state densities. The field-effect mobility monotonically increases with charge density, and exhibits a weak dependence on the permittivity of the polymeric dielectrics, indicative of the delocalized nature of the charge carriers in the oxide semiconductor. Moreover, the low trap state densities, in the region of 10^{12} cm^{-2} eV^{-1}, evidence that the selected polymeric dielectrics are inert with respect to the charge carriers in the oxide semiconductor. This fact is further confirmed by the suitable charge confinement provided by the explored range of polymeric dielectrics under electron accumulation, suggesting a conduction band offset in excess of 1 eV. Remarkably, adequate charge

confinement was observed even for a polymer dielectric with a permittivity as high as 40, thus indicating a way of circumventing the inverse E_G - κ correlation characteristic of inorganic dielectrics and their problematic energy-band alignment with AMOxSs. Finally, the strength of our transistors is demonstrated by their stability under electrical stress, with our best semiconductor-dielectric combinations giving a threshold voltage shift as low as 0.1 V after 14 h stress under demanding constant-current operating conditions.

Our study clearly indicates that organic polymeric dielectrics are an attractive alternative to the inorganic ones for AMOxS-based TFTs. We thus believe that the combination of solution-processed polymeric dielectrics and precursor-based metal-oxide semiconductors have the potential to meet the performance, reliability, and processing challenges of large-area electronics.

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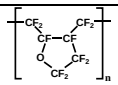
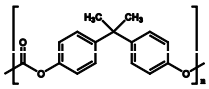
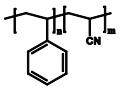
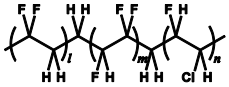
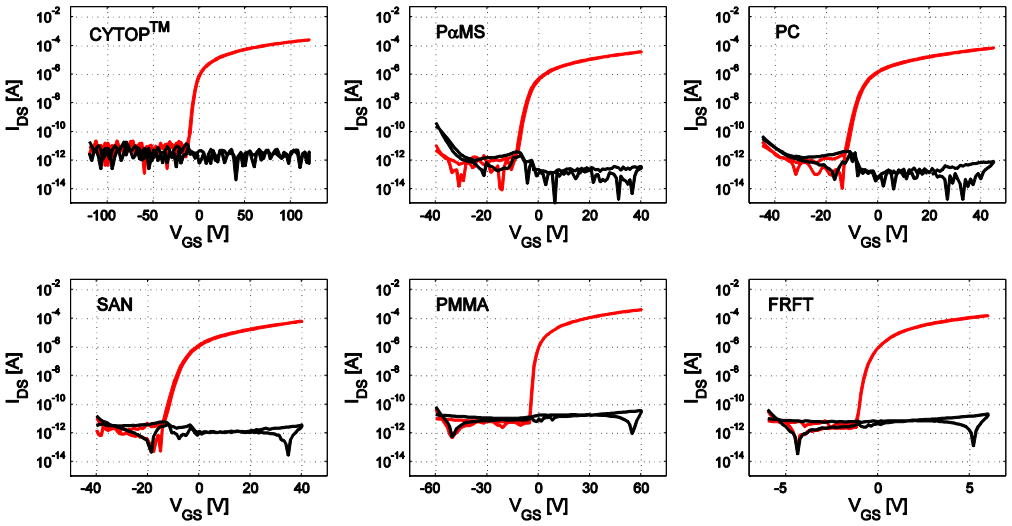
Table 1. Optical gaps and relative permittivities of the selected polymeric dielectrics extracted from the measured data. The repeat units of each of the polymeric dielectrics are also reported.

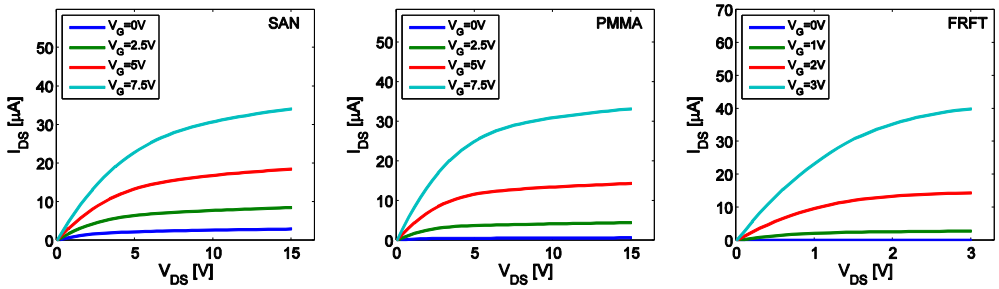
Polymeric Dielectric [units][a)]	Repeat Unit	Optical Gap [eV]	Relative Permittivity[a)]
CYTOP™		> 6	2.1
PαMS		5.09	2.5
PC		4.98	3.2
SAN		5.37	3.4
PMMA		4.92	3.5
FRFT		> 6	40

[a)] Measured at 1 kHz

Figure 1. Linear transfer characteristics (a) of solution-based IZO TFTs utilizing all our polymeric dielectrics, and output characteristics (b) of a representative selection of them.

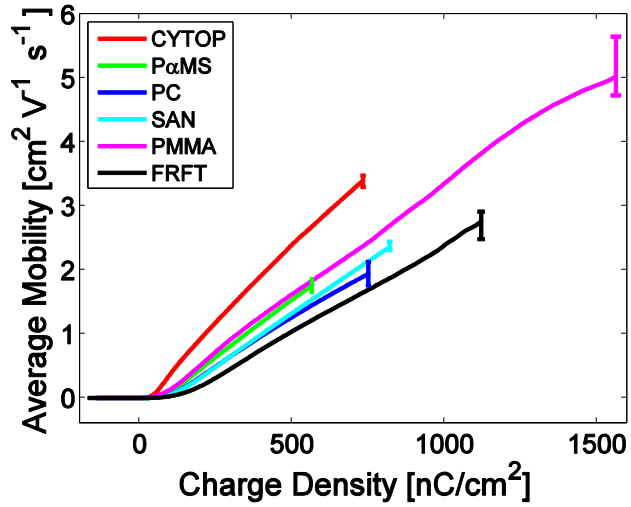


(a)

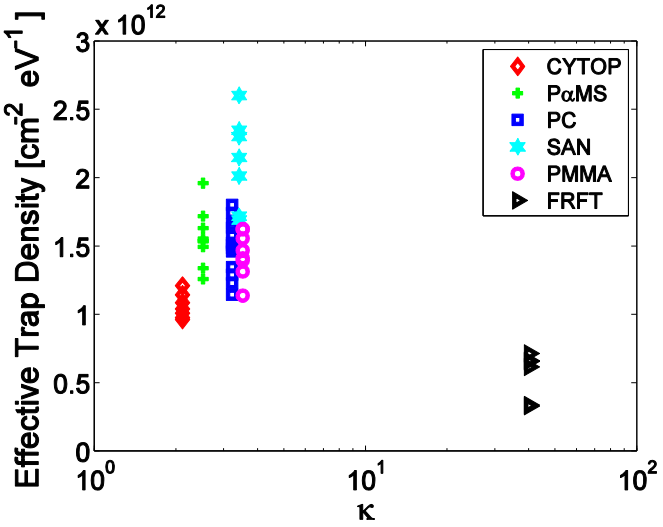


(b)

Figure 2. Average linear mobility versus charge density (a) and effective trap density versus relative permittivity (b) extracted from the transfer characteristics of a number (≈ 10) of IZO devices with each the selected polymeric gate dielectrics. The average mobility is the arithmetic average of the mobility over all samples of each kind, and the error bars indicate the spread at the maximum charge carrier density.

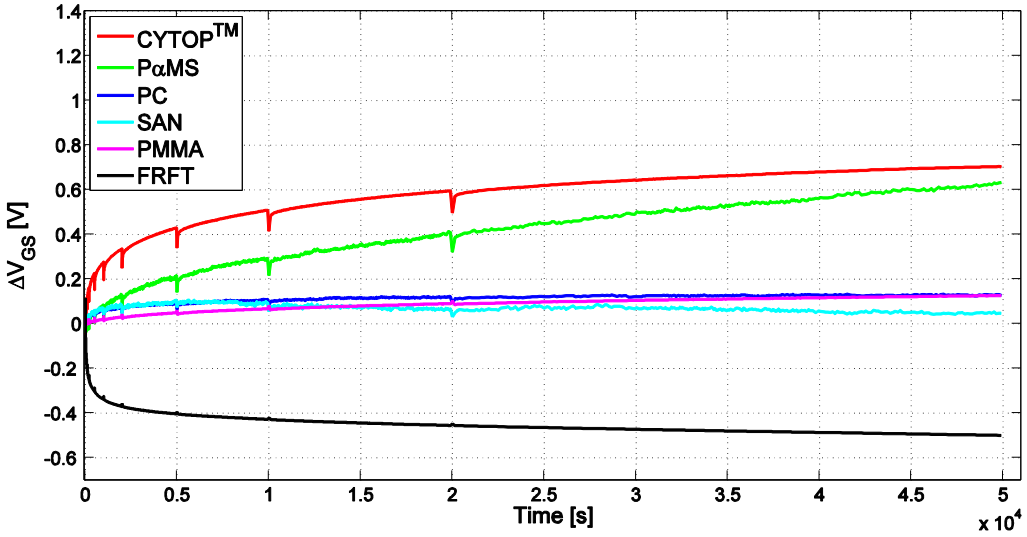


(a)



(b)

Figure 3. Gate-voltage shifts during the constant-current stress experiments presented in this section.



Supporting Information

S.1 UV-vis absorbance of polymeric dielectrics

The UV-vis absorbance behavior of the selected polymers in thin-film form (thickness less than approximately 1μm) is shown in **Figure S1**. Both our fluorinated polymers do not exhibit appreciable absorption in the measured range. As for the other selected polymers, we fitted their absorbance with a power law of the Tauc type: $(h \nu A(\nu))^{1/2} \sim (h \nu - E_g)$, where A is the film absorbance and ν the optical frequency. A good fit of the measured data was obtained, as shown by the solid green lines in Figure S1, from which we determined the optical gaps listed in Table 1.

S.2 Dielectric Response of FRFT

The dielectric response of FRFT thin films was evaluated both at varying frequency and voltages, as shown in **Figure S2**. The measurement was performed on MIM devices consisting of a 215 nm-thick FRFT film sandwiched between aluminium electrodes. The measured data shows an appreciable dispersion of the dielectric response, and a decay of the polarization at sufficiently high fields.

S.3 Gate Leakage Behavior

The PαMS and PC TFTs are characterized by a slight increase in gate current (also reflected in the source and drain current) for large negative gate voltages (beyond E greater than approximately 2 MV cm^{-1}). In general terms, current through the gate dielectric could arise from a variety of mechanisms. Given the specifics of the observed TFT behavior, we can rule out the migration of ionic impurities, the field-assisted detrapping of charge carriers from the bulk dielectric (Poole-Frenkel emission), and space-charge-limited current, as these mechanisms would yield symmetric gate leakage curves; direct tunneling can also be

excluded, given the thickness of our dielectric films. It is then possible that the measured gate current reflects the charge confinement properties of PC and PαMS with respect to our semiconductor: on the one hand, injection into the dielectric would not occur in electron accumulation because of a large conduction-band offset; on the other, injection would occur for negative gate voltages because the valence-band offset can be overcome at a sufficiently high electric field. In principle, however, charge could also be injected from the electrodes. Specifically, for $V_G < 0$ V, electron injection could occur from the aluminum gate, and hole injection from the gold source and drain. Inspection of the energy-band diagram of the transistor stack (see **Figure S3**), however, makes it obvious that injection from the gate electrode would be unphysical. In fact, if electron injection from the aluminum gate occurred for $V_G < 0$ V, we would also observe injection from IZO in electron accumulation, given that the workfunction of aluminum is roughly the same as the electron affinity of IZO. As for hole injection from the gold source and drain for $V_G < 0$ V, in principle a much higher energy barrier would have to be overcome than for holes from the semiconductor, given that the workfunction of gold is smaller than the ionization potential of IZO (by approximately 2 eV). As holes cannot be accumulated in AMOxSs, we thus speculate that the leakage current for $V_G < 0$ V may be due to holes from the gold source and drain electrodes relying on a stepped injection profile through the interposed IZO film. Finally, Fowler-Nordheim plots of the measured leakage current (see **Figure S4**) show a linear dependence of $\ln(I_G / E_{el}^2)$ versus the reciprocal of the gate electric field $1/E_{el}$, thus confirming the possibility of hole tunneling through a thinned energy barrier (Fowler-Nordheim tunneling) into PαMS and PC.

We conclude that PαMS and PC are both capable of providing the necessary confinement in electron accumulation, thus suggesting a conduction-band offset in excess of 1 eV; the slight rise in gate leakage at large negative gate bias, however, hints at a reduced valence-band offset. Given that their bandgap is in the region of 5 eV, the observed leakage is indicative of

an asymmetric placement of their bands with respect to the semiconductor, with a conduction-band offset larger than the valence-band one.

S.4 Constant-Current-Stress Stability

Here we show the threshold voltage and substreshold slope of our low-κ hybrid devices under the constant-current stress we have reported ~~in Section 3.3~~. The threshold voltage shifts shown in **Figure S5** match closely the gate voltage ones in Figure 3, and no degradation of the subthreshold slope is observed. Conversely, the set of transfer characteristics of the FRFT devices under stress, shown in **Figure S6**, denote an increase of the subthreshold slope, suggesting a different degradation mechanism.

Figure S1. Tauc plots of the selected polymers, with the blue circles obtained from the measured absorbance, and the green lines being the linear fit within the pertinent domain.

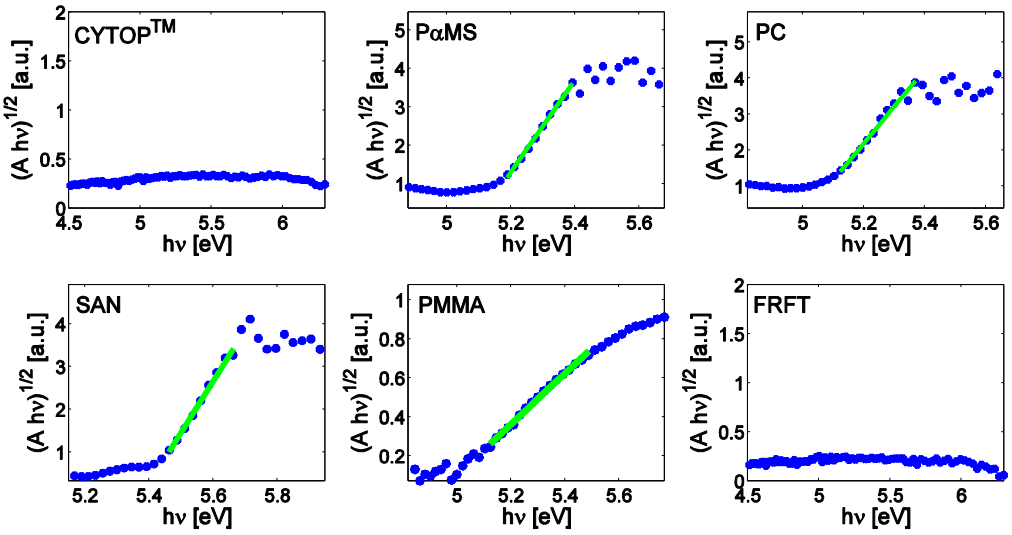
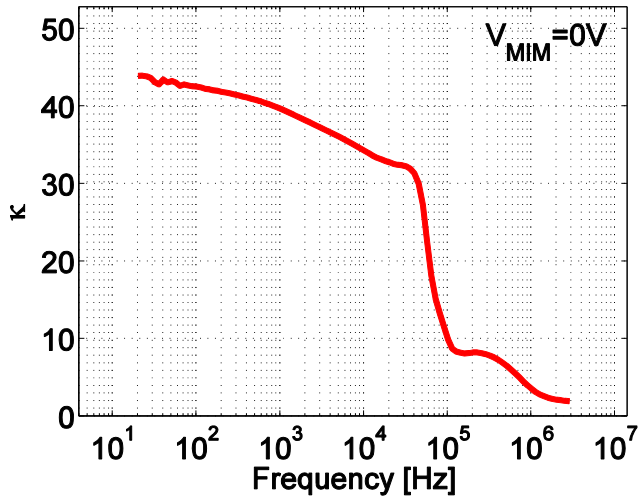
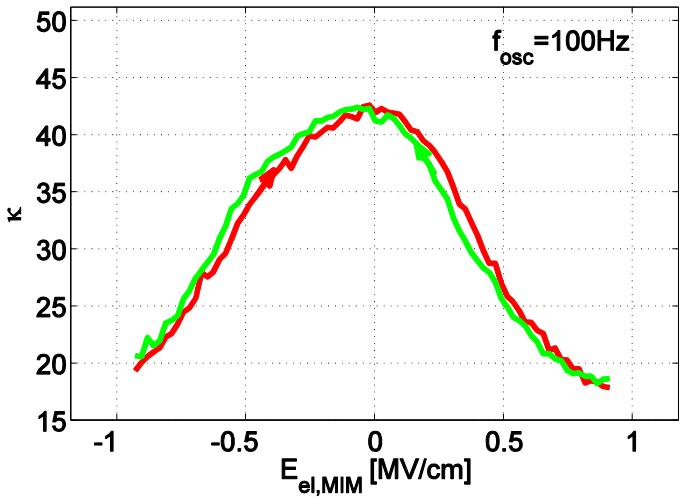


Figure S2. Relative permittivity versus frequency (a), relative permittivity versus electric field (b) of the FRFT. The capacitance versus frequency was measured for a voltage drop of V_{MIM} = 0 V across the MIM devices, and the double-sweep capacitance versus voltage was measured at an oscillation frequency of f_{osc} = 100 Hz (the arrows denoting the direction of the sweep, with the red trace being acquired first)



(a)



(b)

Figure S3. Schematic energy-band diagram of our hybrid TFTs for positive and negative gate voltages. The red arrows indicate the possible pathways for injection into the dielectric. The dashed line for the gold source and drain correspond to the regions where these electrodes overlap with the gate without any semiconductor on top.

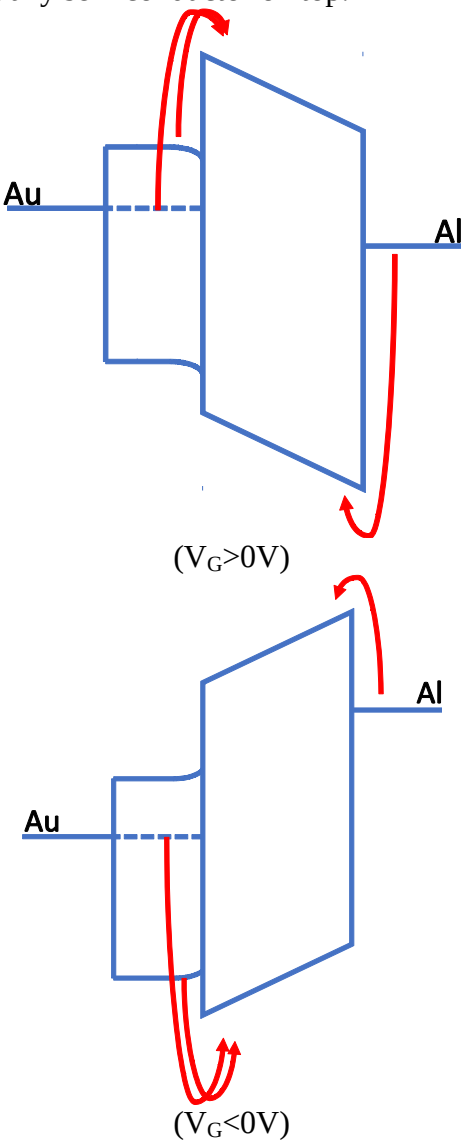


Figure S4. Fowler-Nordheim plots of the gate leakage in a manifold of PαMS and PC TFTs for V_G<0V.

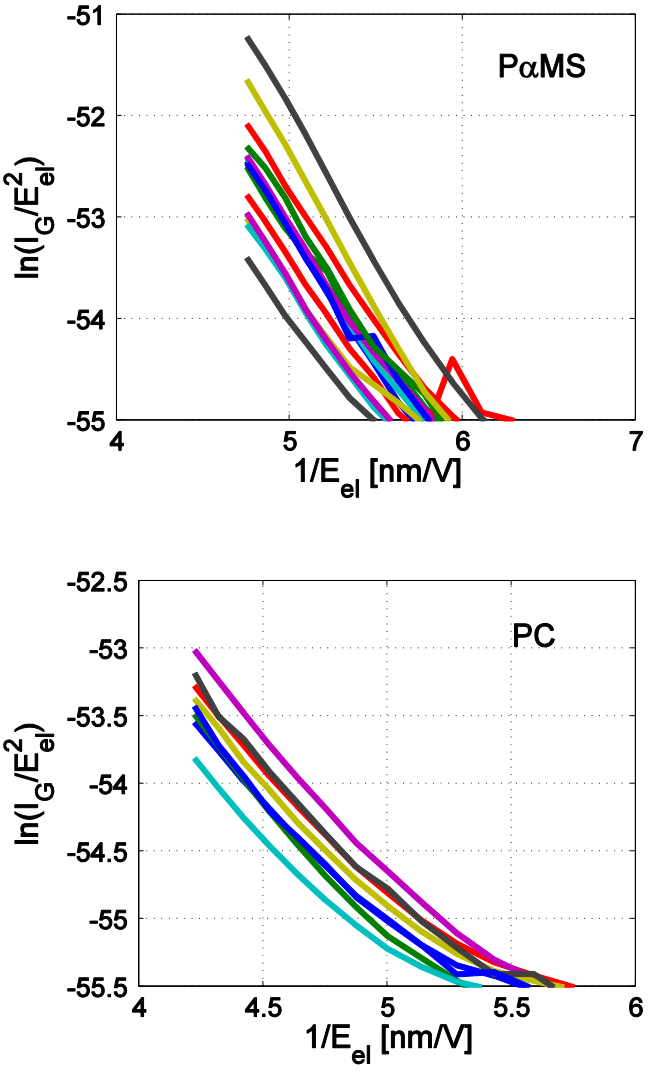


Figure S5. Threshold-voltage shift (on the left) and subthreshold slope (on the right) of our IZO TFTs during constant-current stress experiments with $I_D = 5$ μA.

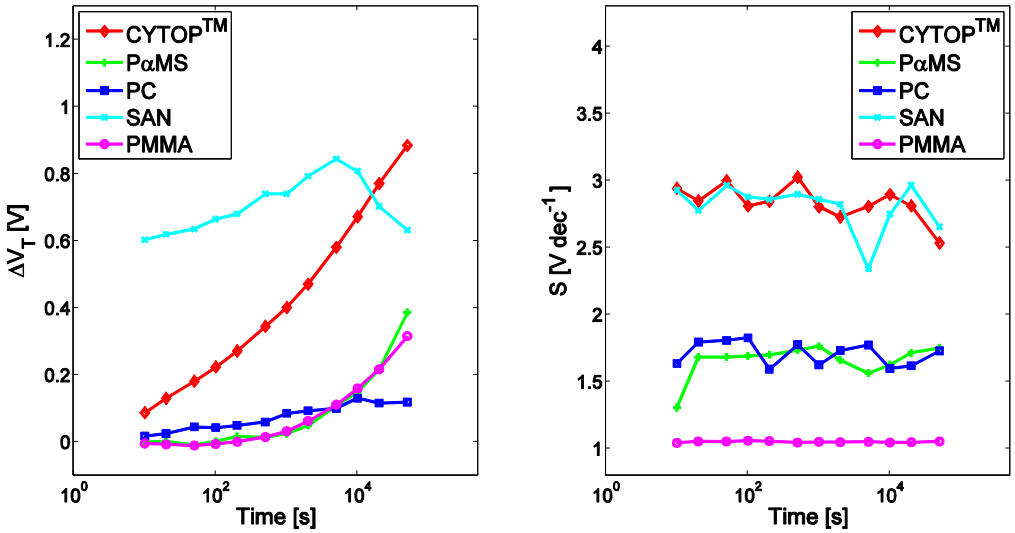


Figure S6. Transfer characteristics of an IZO/FRFT TFT during a constant-current stress experiment with $I_D = 5$ μA.