

Ambipolar Deep-Subthreshold Printed-Carbon-Nanotube Transistors for Ultralow-Voltage and Ultralow-Power Electronics

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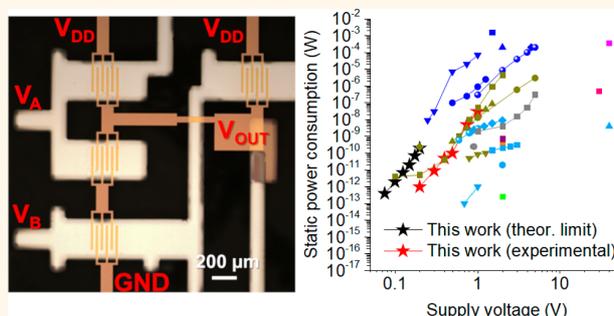
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ABSTRACT: The development of ultralow-power and easy-to-fabricate electronics with potential for large-scale circuit integration (*i.e.*, complementary or complementary-like) is an outstanding challenge for emerging off-the-grid applications, *e.g.*, remote sensing, “place-and-forget”, and the Internet of Things. Herein we address this challenge through the development of ambipolar transistors relying on solution-processed polymer-sorted semiconducting carbon nanotube networks (sc-SWCNTNs) operating in the deep-subthreshold regime. Application of self-assembled monolayers at the active channel interface enables the fine-tuning of sc-SWCNTN transistors toward well-balanced ambipolar deep-subthreshold characteristics. The significance of these features is assessed by exploring the applicability of such transistors to complementary-like integrated circuits, with respect to which the impact of the subthreshold slope and flatband voltage on voltage and power requirements is studied experimentally and theoretically. As demonstrated with inverter and NAND gates, the ambipolar deep-subthreshold sc-SWCNTN approach enables digital circuits with complementary-like operation and characteristics including wide noise margins and ultralow operational voltages (≤ 0.5 V), while exhibiting record-low power consumption (≤ 1 pW/ μm). Among thin-film transistor technologies with minimal material complexity, our approach achieves the lowest energy and power dissipation figures reported to date, which are compatible with and highly attractive for emerging off-the-grid applications.

KEYWORDS: thin-film transistor, carbon nanotubes, ultralow power, subthreshold, hybrid nanodielectrics



Ultralow-voltage (≤ 0.5 V) and ultralow-power (< 1 nW/gate) thin-film transistor (TFT) electronics based on solution-processable semiconductors (*e.g.*, organics, amorphous metal oxides, carbon nanotubes) is in high demand for many emerging applications, *e.g.*, involving portable/remote devices powered by single-cell printed batteries, radio frequency (RF) harvesters, thin-film solar cells, and compact thermoelectric modules, which often can only provide voltages below ~ 1 V and limited currents.^{1,2} For example, the typical power output of an RF harvester 4 km away from a radio antenna is in the tens of microwatts, and power figures in this range are also available from compact thermoelectric harvesters.^{3,4} In this context, requirements on power consumption and the use of low-complexity circuits (including circuits for power management), along with facile scalable fabrication processes, override conventional circuit performance metrics such as speed, especially for “deploy-and-forget” applications, which involve maintenance-free operation

for the whole lifespan. This has driven worldwide research efforts toward the development of thin-film transistor technologies in line with these voltage and power requirements.^{5–10}

To date, the mainstream approaches to low-power TFT electronics involve the use of either two semiconductors with complementary majority carriers (electrons and holes)^{11–15} or a single semiconductor that is n- and p-type doped.^{16,17} Particularly low power dissipation figures can be inherently achieved through these complementary approaches, which,

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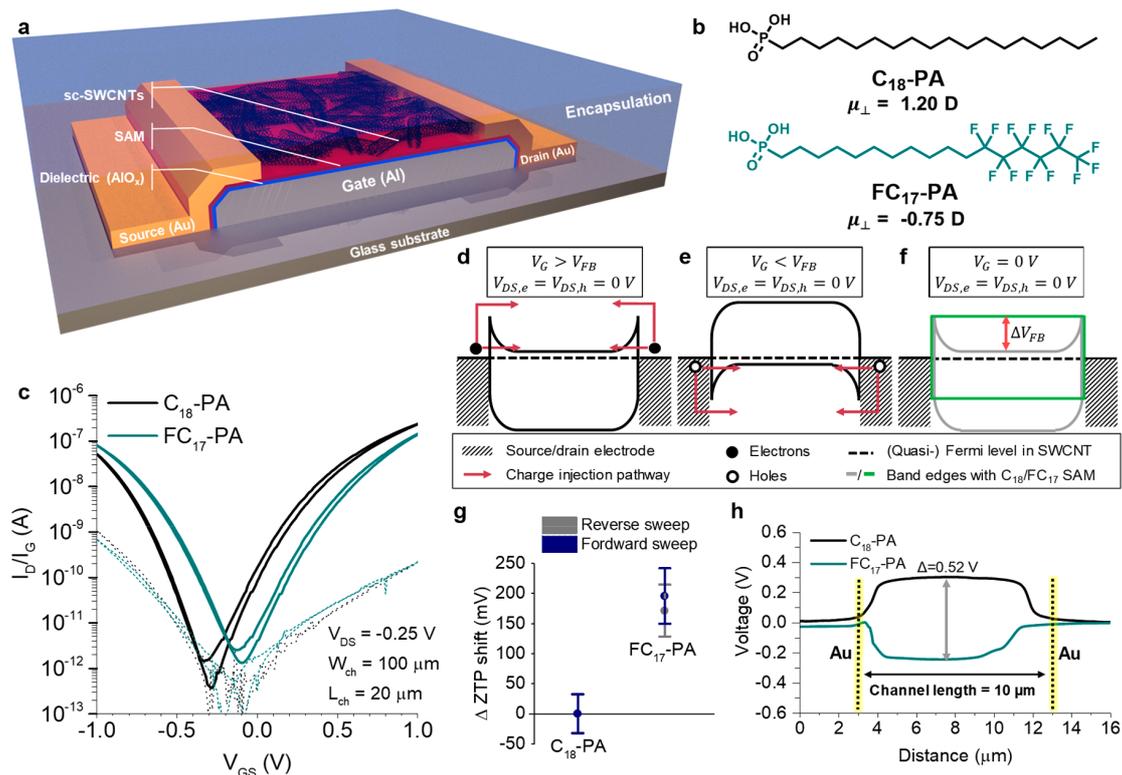


Figure 1. Device architecture, materials, electrical performance, and scanning Kelvin probe microscopy (SKPM) measurements. (a) Structure of the sc-SWCNTN TFTs. (b) C₁₈-PA and FC₁₇-PA SAM molecules and their calculated dipole moments (μ_{\perp}). (c) Exemplary transfer characteristics of sc-SWCNTN TFTs with different nanodielectrics (solid lines) and their corresponding gate leakage currents (dashed lines). (d, e) Schematic energy band diagrams relevant to $V_G > V_{FB}$ and $V_G < V_{FB}$. (f) Effect of a V_{FB} shift (as obtained *via* different SAMs) on the energy band diagram. (g) Relative ZTP shift of devices with FC₁₇-PA nanodielectrics with respect to the C₁₈-PA case; the error bars represent the standard deviation. (h) Surface potential measured *via* SKPM when moving the probe from source to drain over the bare nanodielectrics surface (C₁₈-PA or FC₁₇-PA) without semiconductor material.

however, bring along considerable *material*, *processing*, and *integration complexity*. *Material complexity* is determined by the number of materials in the device stack that need to be deposited. Therefore, within a complementary TFT circuit technology, material complexity pertains to the need of using two different semiconductors and/or dopants, together with source and drain electrode materials with different work functions (*i.e.*, with adequate energy levels to preferentially inject one carrier type or the other¹⁴ and to avoid contact resistance issues and/or the use of high driving voltages). Higher material complexity inevitably lengthens the overall circuit fabrication process (concurrently increasing its cost), due to the number of additional steps required for depositing and/or patterning a larger set of materials. Therefore, regardless of the specific nature of the process steps involved, higher material complexity leads to higher *processing complexity* (which can be quantified in terms of the number of deposition steps and patterning steps required to realize the intended device stack). Additionally, higher material complexity also impacts the complexity of the fabrication process in regard to the alignment overhead, *i.e.*, the need to align each deposition/patterning step with respect to the number of underlying layers. Finally, higher material complexity also increases the overall *integration complexity*, *i.e.*, the need of compensating at a circuit design level for the mismatch in the device characteristics (*e.g.*, mobility and threshold voltage differences, as well as relative variations thereof, between n- and p-channel

transistors), as determined by the use of two different semiconductors and/or two dopants, by alignment errors in their deposition, *etc.* Indeed, the device variability inherently grows with the number of materials to be processed. For example, electronics with particularly low voltage and/or power dissipation figures has been reported based on complementary carbon nanotube-based approaches. These, however, involve high material complexity (*e.g.*, the use of dopants/doping layers and/or different contact materials for source/drain electrodes), which also increases processing complexity (*e.g.*, due to the deposition and patterning of the additional materials).^{14,16,18–30} Such complexity limits the aforementioned target applications and confirms the need to minimize material complexity in order to achieve easy-to-fabricate electronics.

Alternative to the complementary approaches, routes to low-voltage, low-power TFT electronics have been explored in recent years using one single organic/amorphous-metal-oxide semiconductor with unipolar behavior (*i.e.*, conducting only one carrier type).^{7,8,10} However, the unipolar nature of such approaches poses a hurdle in regard to the scalability of the circuit transistor count (as required, *e.g.*, for digital circuits capable of addressing real-world applications) due to the limited/compromised noise margins generally obtained in unipolar integrated circuits.

This work establishes a foundational approach to ultralow-voltage and ultralow-power complementary-like TFT elec-

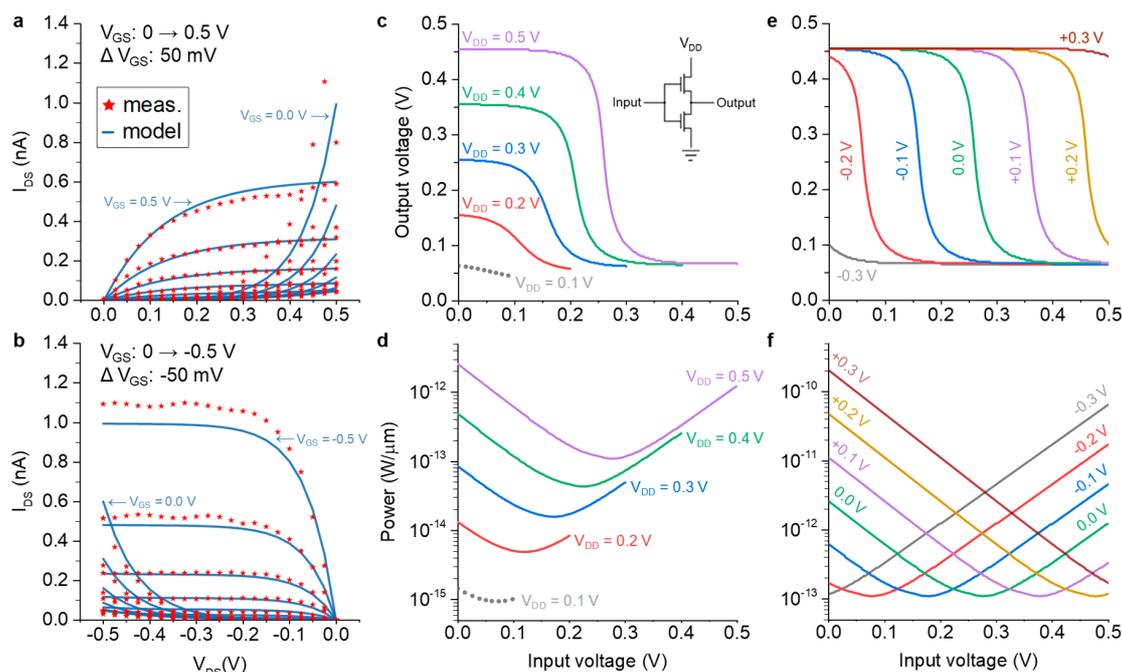


Figure 2. Modeling and simulation of ambipolar deep-subthreshold operation. (a, b) Experimental and modeled output characteristics of an FC₁₇-PA TFT. (c) Inverter voltage-transfer characteristic (VTC) (simulated) at variable V_{DD} (inset: schematic). Dotted curves correspond to VTCs with gain <1. (d) P_s (simulated) corresponding to the VTCs in C. (e) Inverter VTCs (simulated) in the presence of a V_{FB} shift (by the amount indicated near each trace) of the component transistors with respect to 0 V. (f) P_s (simulated) corresponding to the VTCs in (e).

tronics relying on a single pristine (*i.e.*, undoped) semiconductor, namely, printed polymer-sorted semiconducting single-walled carbon nanotube networks (sc-SWCNTNs). Building on their narrow bandgap and inherent charge transport properties, sc-SWCNTNs are employed as the active material of TFTs designed to operate in ambipolar deep-subthreshold mode. The use of only one undoped semiconductor (*i.e.*, sc-SWCNTNs) and one single metal for source/drain electrodes (compare with the material complexity of known complementary approaches) enables minimal material complexity (essential for easy-to-fabricate electronics), allowing the manufacturing of complementary-like circuits with the same number of process steps required for the fabrication of a single transistor. In addition to its minimal material complexity, this approach is able to deliver ultralow-voltage and ultralow-power circuit operation, with supply voltages of ≤ 0.5 V and power dissipation < 1 nW per gate. Key to this outcome is the fine-tuning of the transistor flatband voltage V_{FB} , attained through self-assembled monolayers (SAMs) incorporated in hybrid nanodielectrics. Detailed modeling and analysis provide insight into the underlying working mechanism and the potential of ambipolar deep-subthreshold sc-SWCNTN electronics. The attained reduction of 3 to 5 orders of magnitude in circuit power dissipation—with respect to the prior state-of-the-art ultralow-voltage (power supply ≤ 0.5 V) solution-processable technologies with comparable material complexity—constitutes an important step in the development of ultralow-power electronics compatible with the energy and power demands of emerging off-the-grid applications.

RESULTS AND DISCUSSION

Fabrication and Characterization of Ambipolar sc-SWCNTN TFTs.

Given its direct impact on the subthreshold

swing (SS) (S11), we envisioned that a high-capacitance gate dielectric would be advantageous for sc-SWCNTN TFTs intended for deep-subthreshold operation. In order to realize a high-capacitance dielectric within a bottom-gate top-contact TFT architecture (Figure 1a), we first evaporated an aluminum (Al) gate electrode and subsequently exposed it to oxygen plasma, thus achieving a ~ 3 nm thick alumina (AlO_x) overlayer.¹⁵ A SAM consisting of C₁₈-PA or FC₁₇-PA (Figure 1b) was then solution-deposited on the AlO_x surface,^{15,31,32} resulting in robust AlO_x /SAM nanodielectrics: capacitance $C_{\text{ox-SAM}} > 0.5 \mu\text{F}/\text{cm}^2$ (at 1 kHz) and leakage current $< 1 \mu\text{A}/\text{cm}^2$ (at 0.5 V) (S12). An sc-SWCNT ink^{33,34} was then deposited and patterned by aerosol-jet printing (AJP) to form the semiconducting layer. The ink concentration was fine-tuned empirically by assessing the device performance (Tables S1, S2), so that a suitable sc-SWCNTN (S120) was deposited in a single printing pass. Finally, source/drain electrodes made of one single metal (gold) were patterned onto the sc-SWCNTN, followed by the blanket deposition of a polymer layer for encapsulation. It is noteworthy that this fabrication process is technologically attractive due to its minimal material complexity, as it relies on only one single semiconductor, in its pristine form (*e.g.*, without dopants) and deposited in one single solution-based step, and one single conductive material (and one single deposition/patterning step thereof) for source/drain electrodes.

The resulting sc-SWCNTN TFTs were characterized in air, manifesting good stability for at least 1 month (S13). Additionally, the effect of a prolonged bias stress on the ZTP was found to be of negligible magnitude (S121). Representative characteristics of TFTs with C₁₈-PA- and FC₁₇-PA-based nanodielectrics are shown in Figure 1c. Both devices exhibit an ambipolar behavior with steep and symmetrical SS values (~ 150 mV/decade), ON mobilities of

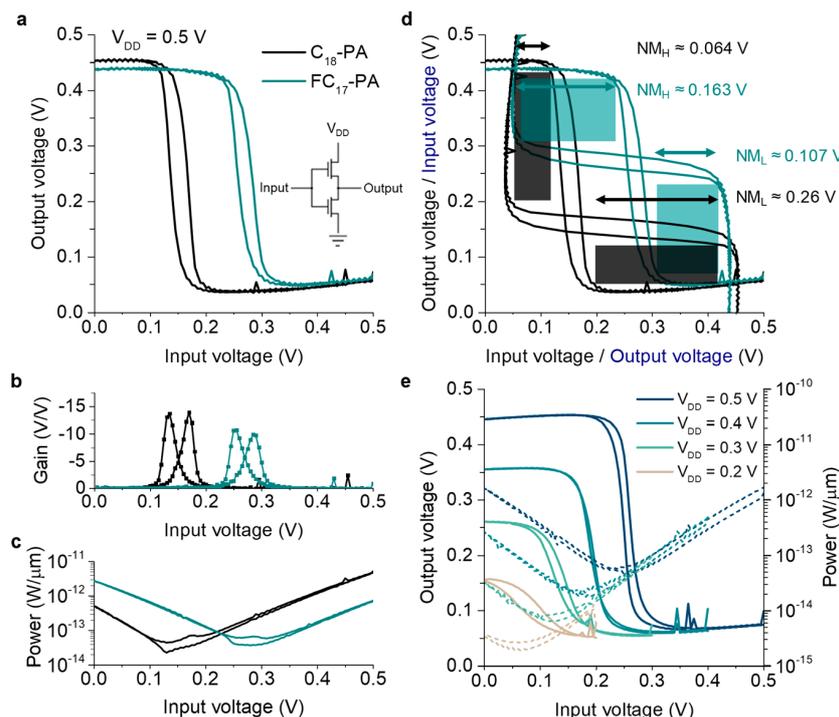


Figure 3. Inverter characteristics. (a) Measured VTCs of sc-SWCNTN TFTs ($W = 100$, $L = 20 \mu\text{m}$) inverters incorporating C_{18} -PA- and FC_{17} -PA-based nanodielectrics. (b–d) Corresponding gain, P_s , and NMs. (e) Measured VTCs and P_s of an inverter with balanced characteristics at variable V_{DD} .

$\sim 8 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and threshold voltages $V_T \approx \pm 0.7 \text{ V}$ (S14, S15). The observed ambipolarity primarily arises from the narrow bandgap ($\sim 0.6 \text{ eV}$) of sc-SWCNTs.³⁵ This enables the facile injection of both carrier types as the gate voltage is raised above (n-channel) or below (p-channel) V_{FB} (Figure 1d,e), provided that the work function of the source/drain electrodes ($\sim 4.9 \text{ eV}$) is similar to that of the sc-SWCNTN ($\sim 4.7 \text{ eV}$).^{36,37} Apart from a matching functional dependence on V_G , the characteristics in Figure 1c exhibit a difference in their zero transconductance points (ZTPs) (the points where $dI_D/dV_G = 0 \text{ S}$). Their ZTPs are separated by $\sim 200 \text{ mV}$, with C_{18} -PA devices exhibiting more negative values than the FC_{17} -PA counterpart. This ZTP shift is in good agreement with the V_{FB} shift (Figure 1f,g) measured *via* scanning Kelvin probe microscopy (Figure 1h) (S16), indicating that transport/trapping effects have only limited impact on the ZTPs (S17, S18b). In turn, the V_{FB} shifts are enabled by the difference in SAM dipole moment (Figure 1b), as evidenced by the close agreement with density functional theory calculations (S17). All this establishes that, by acting on the V_{FB} , SAM nanodielectrics enable the fine-tuning of the current–voltage characteristics of ambipolar sc-SWCNTN TFTs operating in deep subthreshold ($|V_G| \leq 0.5 \text{ V}$).

While previous studies have reported the use of SAMs for the threshold voltage tuning of organic TFTs, in fact, the reported shifts were either more pronounced ($\sim 1.5 \text{ V}$)^{31,38} or of a greater magnitude (in the several tens of volts), all this fuelling the controversy on the underlying mechanism (dipole moment, electronic coupling, charge trapping).^{39–41} As to sc-SWCNTN TFTs, Schießl *et al.* and Vosgueritchian *et al.* reported either that SAM nanodielectrics produce no noticeable shift or that the shifts are of unclear origin and no specific use.^{42,43} Therefore, our experimental findings establish

a direct link between the characteristics of sc-SWCNTN TFTs and the dipole moments of the SAM employed in their nanodielectrics. It is noteworthy that, without encapsulation, our SAM-nanodielectric TFTs do not manifest any noticeable ZTP shift. This highlights the importance of eliminating the influence of environmental factors in order to control precisely the electronic properties of sc-SWCNT TFTs. Similarly, the encapsulant should not “dope” the sc-SWCNTs,⁴⁴ as in fact we confirmed by comparing encapsulated and vacuum-measured nonencapsulated devices (S19).

Modeling of Ultralow-Power Ambipolar Inverters.

Analysis of our ambipolar deep-subthreshold TFT characteristics reveals that the channel current can be expressed as the superposition of an electron current I_e and a hole current I_h (S18a), each individually manifesting an exponential dependence on gate (V_G) and drain (V_D) voltages (e.g., $I_e = I_{0,e} \exp((V_G - V_{FB})/S_{G,e})(1 - \exp(-V_D/S_{D,e}))$, $I_{0,e}$ being a prefactor, $S_{G,e}$ the gate subthreshold slope for electrons, and $S_{D,e}$ the drain subthreshold slope for electrons). Our model equations (S18a) fit the measured current–voltage data (e.g., Figure 2a and b).

The output characteristics of ambipolar deep-subthreshold sc-SWCNTN TFTs using an FC_{17} -PA-based nanodielectric (Figure 2a and b) exhibit a strong similarity to those of p- and n-channel TFTs of an ON (*i.e.*, $|V_G| > |V_T|$) complementary technology. We thus conjectured that, by connecting two such ambipolar deep-subthreshold TFTs in conventional CMOS fashion, it would be possible to achieve complementary-like inverter functionality. Indeed, our simulations building on the aforementioned model equations and on experimental sc-SWCNTN TFT data predict that inverters with a gain greater than unity could be obtained with a supply voltage down to $V_{DD} = 0.2 \text{ V}$ (Figure 2c) with switching thresholds of $\sim V_{DD}/2$

and output voltage swings down to a subthreshold slope away from the power rails (SI10). Our simulations additionally reveal that (a) the static power consumption P_s would decrease (exponentially) to lower levels as V_{DD} is reduced (Figure 2d) and (b) balanced deep-subthreshold ambipolarity ($S_{G,e} \cong S_{G,h}$, $S_{D,e} \cong S_{D,h}$, $I_{0,e} \cong I_{0,h}$, and $V_{FB} \cong 0$ V) is key to minimizing power dissipation (compare with unbalanced deep-subthreshold ambipolarity of the C_{18} -PA-based devices in Figure 1c; see also SI11, SI12). This is clearly evidenced by the inverter simulations in Figure 2e,f, in which a V_{FB} shift in the component transistors dramatically increases power consumption and compromises the noise margins (NMs). In fact, our simulations also allow us to predict the impact of device parameter mismatches (e.g., in V_{FB} and in electron and hole subthreshold slopes; see SI13, SI14) and variability (SI15), hence providing insight into the tolerances of ambipolar deep-subthreshold circuits. Lastly, we pondered if other inverter configurations (i.e., configurations alternative to the complementary-like one discussed up to this point) could be also pursued with our TFTs. To this end, we simulated circuits in which our TFTs are connected in a unipolar logic manner (e.g., in a configuration featuring a zero- V_{GS} load or a diode-connected load). However, our simulations indicate that such circuits would not deliver functional inverters (SI22).

Ultralow-Power Logic Gates. Building on these findings, inverters were fabricated with sc-SWCNTN TFTs using an FC_{17} -PA-based nanodielectric. Exemplary experimental data are presented in Figure 3a, b, c, and d. Here we find that the mere adoption of high-capacitance gate dielectrics is not sufficient to deliver ambipolar deep-subthreshold circuit operation. For instance, the two inverter types shown in Figure 3a,d work equally well at V_{DD} values approaching 1 V (above-threshold operation; see SI16), yet it is only through V_{FB} fine-tuning at the 0.1 V level that it becomes possible to adjust VTCs and power dissipation toward deep-subthreshold circuit functionality and optimum performance. This is exemplified by the NMs (Figure 3d) of the inverter featuring a symmetric VTC (Figure 3a), which are significantly larger than the NMs of the asymmetric counterpart (Figure 3a), directly resulting from a ZTP shift approaching 0.2 V (Figure 1c), an effect that is even more pronounced at lower V_{DD} (SI12). This proves that, in addition to a high gate-dielectric capacitance, a mechanism to fine-tune the transistor characteristics is necessary for ambipolar deep-subthreshold sc-SWCNTN TFT circuit operation, as indeed we achieved with SAM nanodielectrics.

Inverter characteristics at $V_{DD} = 0.5$ V exhibit a gain of >10 and a sub-nanowatt P_s per inverter (i.e., 20 pW per μm of channel width). To the best of our knowledge, this is the lowest power consumption reported to date for TFT inverters consisting of a single semiconductor material (i.e., with the same/comparable material complexity) that can deliver complementary-like VTCs using a complementary circuit architecture (Table S3).^{7,8,10,14–16,23–25,31,45–51,52–56} As an added advantage, the undesirable Z-shaped VTC characteristic of ambipolar inverters is appreciably reduced when the inverters are driven in the deep-subthreshold regime (SI17). Finally, experimental inverter characteristics at variable V_{DD} (Figure 3e) show that functionality (i.e., gain of >1 , based on minimum functionality criterion, SI8d) is maintained (SI18) down to $V_{DD} = 0.2$ V along with a $P_s \approx \text{fW}/\mu\text{m}$ (consistent with our theoretical analysis, SI8f).

We note that, while the ambipolarity of sc-SWCNTN TFTs has been demonstrated and exploited for circuit integration in a large number of works to date, in fact, this was always in the context of their operation in the ON region (i.e., $|V_{G}| > |V_{T}|$). This has indeed resulted in functional logic gates, yet featuring a static power consumption (Table S3) higher by several orders of magnitude than that achieved here and also presenting undesirable Z-shaped VTCs that deteriorate the overall NMs,^{57–60} ultimately limiting both the integration complexity and manufacturing yield. Additionally, ambipolar circuit integration was also investigated with ambipolar organic semiconductors operated in the ON region, resulting in circuits operating with high power dissipation and high operational voltages.^{61,62} Additionally, the organic route to ambipolar integration has been burdened with unbalanced n- and p-channel performance (e.g., mismatches in SS, mobilities, etc.) as well as the presence of a gap of several volts or tens of volts between the onset voltages for the n- and p-channel operation,^{63–66} this aspect leading investigators to explore more complex schemes to try and suppress ambipolarity altogether.^{63,64} All things considered, ambipolarity has been widely regarded as an undesirable property—thus, to be suppressed—in regard to attaining ultralow-power consumption.^{16,51,63,64,67} Contrary to this widely held view of ambipolarity being synonymous with high power consumption, the approach demonstrated herein establishes that ambipolarity not only can deliver ultralow-power circuit operation (<1 nW/gate) with complementary-like VTCs but is in fact highly desirable for low-voltage operation and whenever the material complexity must be kept at a minimum, as is the case for low-cost and/or fully solution-processed scenarios.

To assess the reproducibility of our approach, we first measured the VTCs and power consumption of 10 inverters, five with C_{18} -PA and five with FC_{17} -PA nanodielectrics (Figure 4a–d). The inverters show a maximum variability of their switching threshold of ~ 100 mV, in agreement with the maximum ZTP deviation already pointed out in Figure 1g. Additionally, we extracted the distribution of the SS from the measured characteristics of 18 TFTs for each SAM nanodielectric (Figure 4e). We note that the observed level of variability is common when conducting prototype device fabrication in a research laboratory. The slight difference in SS between the two device types can be accounted for in part by the difference in areal capacitance of the corresponding nanodielectrics (SI2) and in part by slight differences in interfacial trap densities (Table S1) (likely influenced by the SAM chemistry). In order to evaluate the impact of such experimental SS variability on inverter functionality, we conducted Monte Carlo simulations incorporating the SS variability derived from our TFT measurements. The simulated inverter variability (SI15) captures well the experimental inverter variability (Figure 4e). Therefore, Monte Carlo simulations also confirm that the device-to-device variability of our TFTs does not impinge on their ambipolar deep-subthreshold circuit operation with ultralow-power characteristics (SI15).

In addition to assessing its robustness against device parameter variability, we also evaluated the scalability of our approach to more complex circuits by pursuing the integration of NAND gates. The significance of such kind of digital gates derives from their universal character, insofar as NAND gates can be used as the building block for digital circuits of arbitrary function and complexity.⁸⁸ We found that our approach is

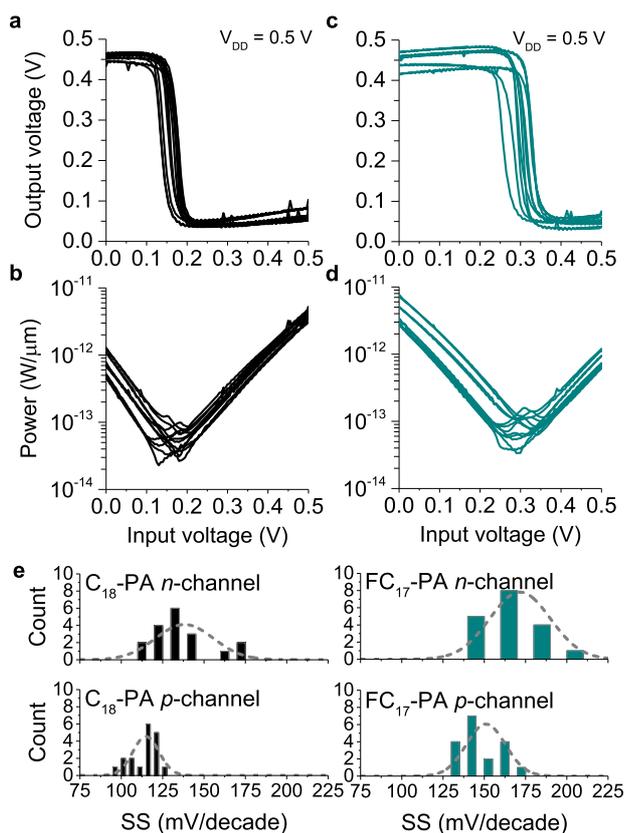


Figure 4. Experimental assessment of circuit and device reproducibility. (a) Measured VTCs of five inverters based on the C_{18} -PA nanodielectric and (b) their corresponding power dissipation. (c) Measured VTCs of five inverters based on the FC_{17} -PA nanodielectric and (d) their corresponding power dissipation. (e) SS distributions extracted from the measured characteristics of 18 devices with C_{18} -PA and FC_{17} -PA nanodielectrics.

capable of delivering NAND functionality with ultralow-voltage and ultralow-power characteristics, as shown in Figure 5. Indeed, NANDs built with our ambipolar deep-subthreshold sc-SWCNT TFTs in a CMOS-like configuration can operate down to $V_{DD} = 0.3$ V and with maximum power consumption $\max(P_s) < \text{pW}/\mu\text{m}$ (Figure 5a and b), an unprecedented level for such circuits based on ambipolar TFTs (Table S3). Considering its robustness against device parameter variations and its capability to deliver universal NAND gates, the proposed ambipolar deep-subthreshold SWCNT-based integrated circuitry offers a reliable platform for the future development of circuits of higher complexity with ultralow-voltage and ultralow-power characteristics.

Status and Outlook for Ultralow-Voltage, Ultralow-Power TFT Electronics. To appreciate the significance of our findings, it is useful to compare our approach with other technologies based on solution-processable semiconductors (sc-SWCNTs, amorphous metal oxides, and organic semiconductors) reported in the literature. For this purpose, we illustrate in Figure 6a all pertinent works—to the best of our knowledge—that report supply voltage and power dissipation figures. We find that, in the ultralow-voltage region ($V_{DD} \leq 0.5$ V), our approach delivers the lowest power dissipation of all technologies (complementary, unipolar, and ambipolar). In

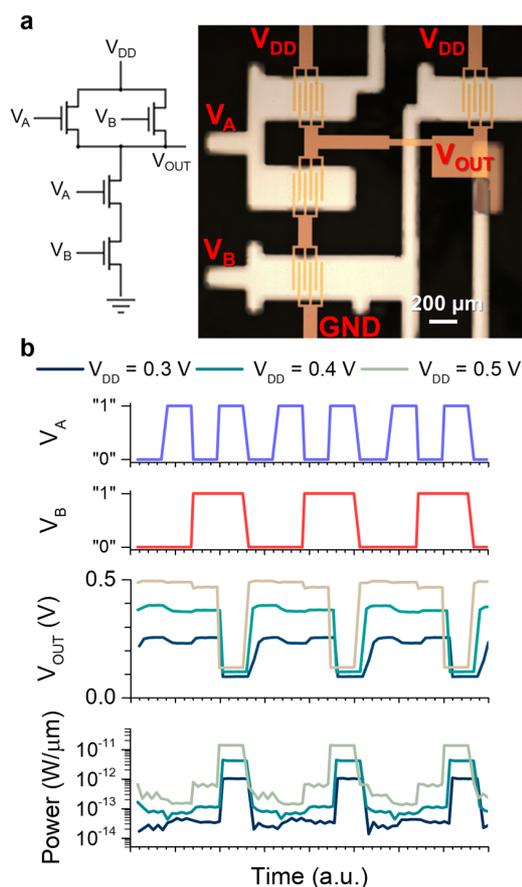


Figure 5. NAND gate characteristics. (a) Schematic and micrograph of an ambipolar deep-subthreshold NAND. (b) Measured characteristics and P_s of a NAND. “1” and “0” correspond to V_{DD} and GND in all cases. The time is specified in arbitrary units because the measurement is dependent on the integration times of the semiconductor parameter analyzer.

regard to technologies of comparable material complexity—a key aspect for easy-to-fabricate electronics—and ultralow-voltage capability, our work attains a reduction of 3 to 5 orders of magnitude in power dissipation (compare with the power dissipation of unipolar and ambipolar technologies, *i.e.*, technologies of material complexity comparable to our approach).

Furthermore, our analysis suggests that ambipolar deep-subthreshold sc-SWCNT circuits could potentially function at even lower V_{DD} and power dissipation. To investigate this possibility, we simulated inverters based on experimental parameters from sc-SWCNT TFTs (comprising FC_{17} -PA-based nanodielectrics) except for the SS being set to its theoretical limit, *i.e.*, 60 mV/decade (S18a). This limit could be approached in the future by further increasing the gate dielectric capacitance (*e.g.*, via shorter SAM molecules and/or by replacing the AlO_x with higher- k oxides of similar thickness) and/or by reducing the interfacial trap density (*e.g.*, by changing the chemistry of the SAM in the hybrid nanodielectric). The corresponding simulated VTCs (Figure 6b) show that such inverters could operate (Figure 6c; see minimum functionality criterion in S18d) with a V_{DD} down to ~ 0.075 V, while dissipating in the $\text{fW}/\mu\text{m}$ range (Figure 6d). Being more compromising with power consumption, a

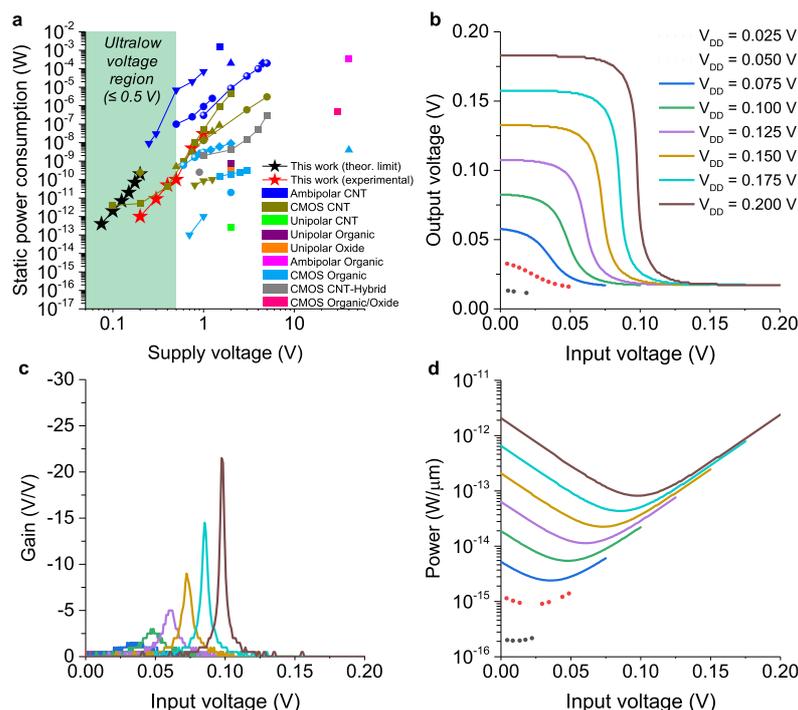


Figure 6. Perspective on ambipolar deep-subthreshold sc-SWCNTN circuits. (a) Inverter supply voltage vs static power consumption of our theoretical (black stars) and experimental work (red stars) compared to literature reports to date (Table S3). (b) Calculated VTCs of an ambipolar deep-subthreshold inverter comprising sc-SWCNTN TFTs with an ideal SS (60 mV/decade). Dotted curves correspond to a gain of <1 . (c) Associated gain. (d) Associated P_s .

better performance can be anticipated, e.g., a gain of >20 for $V_{DD} = 0.2$ V and $P_s \approx \text{pW}/\mu\text{m}$. In fact, apart from enabling lower V_{DD} and P_s , a reduction in SS would lead to ambipolar deep-subthreshold sc-SWCNT circuits with higher noise immunity (i.e., NMs), as it would enable an exponential increase in gain and an output swing closer to ideal (i.e., rail-to-rail) (SI8c, SI8e, SI19). Finally, while additional effects (such as Schottky barriers at the semiconductor–metal interfaces) may prevent the aforementioned thermodynamic limit from being reached, Figure 6a shows that SS values intermediate between our present results and the thermodynamic limit (as could be achieved with the strategies presented earlier) would nonetheless deliver logic gates statically dissipating in the 10 fW/ μm to 1 pW/ μm range with a supply voltage in the range of 0.1–0.2 V.

CONCLUSION

In summary, we have demonstrated the use of ambipolar deep-subthreshold sc-SWCNTN TFTs comprising hybrid nanodielectrics for ultralow-voltage (≤ 0.5 V) and ultralow-power (10^{-15} – 10^{-12} W/ μm per gate) complementary-like circuits. Overcoming the commonly held view that ambipolarity is synonymous with high power dissipation, here our approach to ambipolar transistors proves key to achieving ultralow-power operation, along with complementary-like circuit characteristics. Importantly, this is achieved with a minimal set of materials, consisting of just one single undoped semiconductor and one single material for source and drain electrodes. An essential enabler of this approach is the ability to fine-tune the TFT V_{FB} , achieved here with SAM nanodielectrics. Compared to other TFT technologies based on solution-processable semiconductors (sc-SWCNTs, amorphous metal oxides, and

organics) of similar material complexity and operating at ultralow voltages ($V_{DD} \leq 0.5$ V), our approach delivers a reduction in power dissipation by 3 to 5 orders of magnitude.

Looking ahead, further improvement on our performance figures would be possible (e.g., targeting inverter gate operation with $V_{DD} \approx 0.1$ – 0.2 V and $P_s \approx 10$ fW/ μm to 1 pW/ μm) by pushing the SS toward its theoretical limit. In fact, on the basis of our current experimental results, it can be envisaged that complex ambipolar deep-subthreshold sc-SWCNTN circuits could be powered throughout their entire lifetime by low-cost single-cell disposable batteries or by energy harvesters, eliminating the need for complex power management circuitry (battery chargers, charge pumps, DC/DC converters, etc.). Taking into account the current experimental state of this work and considering the current state of energy harvesting technologies^{3,4} (e.g. RF, thermoelectric), circuits of complexity equivalent to tens of thousands of NAND gates (e.g., more than enough for 125 8-bit full-adders) could comfortably be powered continuously with a single-cell thin-film disposable battery or energy harvester. For instance, a thin-film solar cell with an efficiency on the order of 10% would only require an area of $100 \times 100 \mu\text{m}^2$ to meet the power demand of such circuits. In conclusion, the ambipolar deep-subthreshold sc-SWCNTN TFT approach presented here constitutes an important breakthrough enabling the development of electronics compatible with the energy and power demands of the emerging off-the-grid and “deploy-and-forget” applications.

MATERIALS AND METHODS

The materials employed in this work were used as received and without further purification, unless specified otherwise. Toluene

(CAS: 108-88-3), trifluorotoluene (CAS: 98-08-8), 2-propanol (CAS: 67-63-0), *n*-butyl acetate (CAS: 123-86-4), and *n*-methyl-2-pyrrolidone (CAS: 872-50-4) were purchased from Sigma-Aldrich (USA). The octadecylphosphonic acid (C_{18} -PA) molecule was bought from Sigma-Aldrich (USA), whereas the (12,12,13,13,14,14,15,15,16,16,17,17,17-tridecafluoroheptadecyl)phosphonic acid (FC_{17} -PA) molecule was bought from Sikemia (France). Poly(methyl methacrylate) (PMMA) ($M_w \approx 120\,000$) (CAS: 9011-14-7) was purchased from Sigma-Aldrich (USA). The Parylene-C precursor Galxyl C was purchased from Galentis (Italy). The isoindigo-based poly(9,9-dioctylfluorene) (PFO) derivative (PFIID) was synthesized in our laboratories as described in an earlier report.³³ P2 single-walled carbon nanotubes by arc discharge were purchased from Carbon Solution (USA). LOR5B (resist), S1813 (photoresist), and MF319 (developer) were purchased from Microchem-Kayaku Advanced Materials (USA).

TFT Fabrication. Gate Electrode and Hybrid Nanodielectric Deposition. Thirty-nanometer-thick high-purity (99.99%) Al gate electrodes were thermally evaporated onto glass substrates through a shadow mask under high vacuum ($<2.0 \times 10^{-6}$ mbar). The samples were then treated with oxygen DC plasma (140 W for 5 min in a vacuum of 0.2 mbar) so as to form an AlO_x layer over the Al electrodes. Afterward, the samples were immersed overnight (>16 h) in a solution consisting of a single or a stoichiometric mix of phosphonic acid molecules dissolved in 2-propanol (0.2 mM in all cases) so as to form a SAM on the AlO_x overlayer. Finally, the samples were rinsed vigorously with neat 2-propanol, dried under nitrogen flow, and annealed at 70 °C for 5 min so as to remove excess solvent.

Printing of sc-SWCNTs. The sc-SWCNT ink was deposited via AJP (Optomec, USA) atop a freshly SAM-modified AlO_x/Al stack with a printing speed of 1.5 mm/s. Samples were then annealed at 120 °C for 10 min (in air). Subsequently, excess polymer and sc-SWCNTs were washed away by gently rinsing in neat toluene. Lastly, substrates were dried under nitrogen flow and annealed at 120 °C for 10 min (in air) so as to remove excess solvent.

Fabrication of Source and Drain Electrodes. Thirty-nanometer-thick high-purity (99.99%) Au source and drain electrodes were deposited via thermal evaporation and patterned via standard double-layer lift-off photolithography (based on LOR5B and S1813 resists).⁶⁹ The resulting source and drain electrodes defined a channel geometry with width $W_{ch} = 100\ \mu\text{m}$ and length $L_{ch} = 20\ \mu\text{m}$, or with $W_{ch} = 1000\ \mu\text{m}$ and $L_{ch} = 20\ \mu\text{m}$.

Device Encapsulation. The first step of the encapsulation process was carried out in a nitrogen-filled glovebox. There, devices were annealed on a hot plate at 200 °C for 3 h. Subsequently, devices were coated with a 180 nm thick PMMA layer, deposited via spin coating (2000 rpm) from a 40 g/L solution in anhydrous *n*-butyl acetate. Devices were then annealed at 90 °C for 30 min to remove excess solvent. Afterward, devices were transferred to an adjacent parylene coater (Penta Technology, China) (exposure to air <1 min). There, the final encapsulation step was carried out, involving the deposition of 600 nm thick Parylene-C films.

SAM Solution Preparation. The C_{18} -PA solution was prepared by dissolving 2.0 mg of C_{18} -PA in 30 mL of 2-propanol (0.2 mM). The FC_{17} -PA solution consisted of 3.3 mg of FC_{17} -PA dissolved in 30 mL of 2-propanol (0.2 mM). The 1:1 C_{18} -PA: FC_{17} -PA solution consisted of a mixture of 15 mL of the 0.2 mM C_{18} -PA solution and 15 mL of the 0.2 mM FC_{17} -PA solution. Finally, all solutions were placed in closed containers and in an ultrasonic bath for at least 15 min to ensure the complete solvation of the phosphonic acid molecules.

Capacitor Fabrication. Capacitors were fabricated for the characterization of the hybrid oxide/SAM nanodielectrics. A micrograph of the final capacitor structure is shown in (SI2). Such capacitors were fabricated as follows.

Bottom Electrode and Hybrid Nanodielectric Deposition. Al electrodes and SAM/ AlO_x were deposited according to the same procedure detailed in TFT Fabrication (see Gate Electrode and Hybrid Nanodielectric Deposition subsection).

Top Electrode Deposition. Thirty-nanometer-thick high-purity (99.99%) Au gate electrodes were thermally evaporated through a shadow mask and in high vacuum ($<2.0 \times 10^{-6}$ mbar).

sc-SWCNT Ink Preparation. The sc-SWCNT ink consisting of (16,2) semiconducting carbon nanotubes was synthesized by adding 10 mg of arc discharge carbon nanotubes (Carbon Solution, USA) and 5 mg of PFIID to 20 mL of toluene.³⁴ The mixture was then subjected to probe ultrasonication for 30 min at 0 °C (Sonics & Materials Inc., VCX 130 60 W, USA), allowing the PFIID polymer to selectively wrap around sc-SWCNT, rendering them highly soluble in toluene.³⁵ Subsequently, the homogenized mixture was centrifuged at 30000g for 2 h to remove the fractional amount of metallic carbon nanotubes and any other insoluble material. The supernatant was carefully removed from the centrifuge tube, thus yielding the carbon nanotube ink consisting of (16,2) semiconducting carbon nanotubes.³³ The ink was then characterized via UV-vis-NIR spectroscopy (PerkinElmer, Lambda 750 UV-vis-NIR, USA) to verify that no metallic carbon nanotubes were present in the solution as thoroughly described in previous publications.^{33,48,70,71} The ink was further diluted with toluene in order to have a concentration suitable for AJP. In particular, such dilution resulted in an ink with a maximum absorbance of approximately 0.35 in the region of 800–1200 nm, as measured by UV-vis spectroscopy with the ink placed within a quartz cuvette with a 10 mm optical path. This concentration results in a dense sc-SWCNTN after just one AJP printing step. Because printing onto hydrophobic surfaces with toluene as a solvent is not viable due to dewetting (SI2), half of the solvent (toluene) was evaporated by leaving the ink container open and exposing it to the airflow of a chemical hood. The evaporated toluene was then replaced with the same volume of trifluorotoluene with no impact on the solubility of the sorted sc-SWCNTs. Finally, 50 μL of terpinol per mL of ink was added to the ink in order to facilitate the aerosol-jet printing process.

Dipole Moment Calculations. Dipole moments of C_{18} -PA and FC_{17} -PA were computed based on their geometry-optimized structures of single molecules using density functional theory (DFT) calculations with the program Gaussian 09 suite.⁷² The geometries were optimized using the M06-2X variation of the hybrid functional of Truhlar and Zhao.⁷³ The basis sets 6-31G were employed with connectivity specifications (geom = connectivity). In addition, p-type functions were added on to hydrogens; d-type functions and diffuse functions were added onto all other atoms.

Device Characterization. Devices and circuits (capacitors, TFTs, inverters, NANDs) were characterized inside a Faraday cage, in the dark and in air using a probe station with shielded micromanipulators (equipped with tungsten probe tips). Semiconductor parameter analyzers (either a Keithley 4200-SCS or a Keithley 4200A, Keithley Instruments, USA) were used to conduct most electrical measurements reported in this work. Higher frequency (≥ 1 kHz) capacitance measurements were performed via impedance spectroscopy using a 4200 CVU module embedded within a Keithley 4200-SCS, while the lower frequency (<1 kHz) capacitance measurements were conducted with a Hioki IM3533 LCR meter (Hioki, Japan).

Scanning Kelvin Probe Microscopy (SKPM) Measurements. Samples for SKPM were fabricated with the same structure and through the same process employed for TFT fabrication, except that they did not include any sc-SWCNT. Measurements were carried out with a Cypher S AFM microscope (Oxford Instruments, UK) and relied on platinum-coated silicon probes (ElectriMulti75-G, Budget-Sensors, Bulgaria). During the measurements, gate, source, and drain electrodes were connected to the SKPM system ground. The SKPM probe scanned the area over the sample nanodielectric between source and drain electrodes.

TFT/Circuit Modeling and Simulation. Model parameter extraction and TFT/circuit simulation were conducted in a GNU Octave environment.

sc-SWCNTN Capacitor Fabrication. Capacitors were fabricated for the characterization of the effective gate dielectric capacitance associated with our printed sc-SWCNTN TFTs. A depiction of the capacitor structure is provided in SI2. Such capacitors were fabricated as follows.

Bottom Electrode and Hybrid Nanodielectric Deposition. Al electrodes and SAM/ AlO_x were deposited according to the same procedure detailed in **TFT Fabrication**; see Gate Electrode and Hybrid Nanodielectric Deposition subsection).

Printing of sc-SWCNTs. The sc-SWCNT ink was processed according to the same procedure detailed in **TFT Fabrication** (see Printing of sc-SWCNTs subsection).

Top Electrode Deposition. Thirty-nanometer-thick high-purity (99.99%) Au electrodes were thermally evaporated through a shadow mask in high vacuum ($<2.0 \times 10^{-6}$ mbar).

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsnano.0c06619>.

Additional materials characterization, supporting figures and text (S11–S122), calculation details, and Tables S1–S3 (PDF)

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Author Contributions

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Author Contributions

V.P. and J.Z. proposed and supervised the project. L.P. developed and carried out device and circuit fabrication, characterization, and experimental data analysis. V.P. developed the device and circuit models, simulations, and theoretical analysis. Y.W. and F.L. conducted the SKPM measurements. L.S. performed the dipole moment calculations. R.M. and M.M.W. prepared the sc-SWCNT inks and performed part of the encapsulation process. L.P. and V.P. cowrote the manuscript, and J.Z., L.O., T.D.A., and Z.C. revised it. L.P., V.P., J.Z., L.O., T.D.A., and Z.C. analyzed the data. All the authors discussed the results and commented on the manuscript.

Notes

The authors declare the following competing financial interest(s): A patent application related to the results presented here has been filed by Soochow University with V.P., L.P., and J.Z. as inventors.

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