Air-stable N-type Printed Carbon Nanotube Thin Film Transistors for CMOS Logic Circuits

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Abstract

The lack of long-term air-stable and solution-processed n-doping methods for printed single-walled carbon nanotube (SWCNT) thin film transistors (TFTs) limits their integrations into printed complementary metal-oxide-semiconductor (CMOS) circuits. In this paper, a new chemically modified epoxy amine ink was developed as the chemical dopant and encapsulant to enable the uniform n-type SWCNT-TFTs with long-term air stability (6 months). The epoxy amine inks were dropped onto the printed p-type TFT device channels in a single-step solution process. As a result, printed top-contact n-type SWCNT-TFTs were obtained with well-balanced electrical chararcteristics comparable to their p-type counterparts. The matched p-type and n-type SWCNT-TFTs were thus integrated into the printed CMOS inverters and NAND gates, which have both achieved proper logic operation at supply voltages below 1 V. In particular, the CMOS inverters could operate with V_{DD} down to 0.3V with associated peak power consumption of 0.06 μW, showing full rail-to-rail output swings with voltage gains up to 22, trip voltages of ~V_{DD}/2, and maximum noise margin of 0.42 V at V_{DD} = 1.1 V (~76.4 % of V_{DD}/2). Furthermore, the static characteristics of CMOS inverters could be maintained for 3 months with negligible changes, proving the feasibility of this long-term air-stable n-doping method.

Keywords: Semiconducting single-walled carbon nanotubes (sc-SWCNTs), Printed thin film transistors (TFTs), N-doped, Epoxy resin, Air stability, CMOS logic circuits

1. Introduction

Semiconducting single-walled carbon nanotubes (sc-SWCNT) show excellent chemical and physical stability, high carrier mobility, good solubility, and low processing temperatures. Thus, they have become promising candidates to develop printed thin film transistors (TFTs). In particular, printed TFTs based on semiconducting carbon nanotubes have been explored for many applications, such as integrated circuits[1–3], photodetectors[4], neuromorphic devices[5], pressure sensors[6], active matrix for sensors[7] and electrochromic displays[8]. To achieve low static power consumption and noise-resistant devices essential for the realization of large-scale integrated circuits, logic circuits are typically implemented in the complementary metal oxide semiconductor (CMOS) configuration, consisting of two balanced unipolar n-type and p-type transistors.

Although sc-SWCNT are intrinsically ambipolar, transistors made of sc-SWCNTs usually exhibit p-type characteristics in air due to two reasons: one is the easy adsorption of ambient oxygen and moisture[9] and the other is the uneven electrons and holes charge injection at the source and drain electrodes. Therefore, a number of strategies have been developed to enhance the electrical properties and stability of n-type SWCNT-TFTs for high-performance CMOS logic circuits as well as a modern microprocessor[10,11], such as atomic layer deposition (ALD) of high-κ metal oxides[12–14]/nitrides[15] on sc-SWCNT thin films, low work function source/drain contacts[16,17], and chemical doping, i.e. polyethylenimine[18,19](PEI) or reducing small molecules[20–24].

However, the existing n-type doping strategies for SWCNT-TFTs suffer from environmental instability and/or process complexity, which hinders the realization of large-scale integrated circuits. For example, low work function metals can be easily oxidized in ambient condition. ALD deposited metal oxides or nitrides can provide a good encapsulation which lead to highly air-stable systems[14,15]. Nonetheless, it is not easy to selectively achieve printed n-type TFTs and CMOS circuits by the use of ALD technique. In contrast, chemical doping can be easily implemented due to the solution nature of commonly used chemical dopants. Nevertheless, doping agents (PEI[19] and hydrazine[25]) exhibit most of the time poor environmental stability. Although some progress have been made using air-stable molecules, such as benzyl violene[23], β-Nicotinamide adenine dinucleotide, reduced dipotassium salt (NADH)[26] and ethanolamine (EA)[21], the resulting n-type devices still showed significant performance degradation in air due to the surface adsorption of O_2 and H_2O. To solve this issue, chemical doping combined with ALD encapsulation[19] or top-gate structure[27] have been developed to achieve n-type devices with excellent air stability. Recently, SU-8, an epoxy photoresist[28,29], as both doping and encapsulating material has shown good potential for air-stable n-type SWCNT-TFTs, avoiding the use of complex ALD approach. This n-doping process, originating from crosslinking photoninitiators[28] (Triarylium-solphonium salts), show air stability over 100 days with reasonable ON current degradations for n-type devices[29]. However, it is worth mentioning that long UV exposure might lead to the total conversion of the photon acid generator and thus

to deteriorate performance of the n-type SWCNT devices over time.

In this paper, we report a novel doping approach to obtain printed n-type SWCNT-TFTs with long-term stability in air. An epoxy-based ink was developed as both a doping and encapsulating material, and was simply formulated by mixing an epoxy resin with a crosslinking agent containing n-doping amine groups. As-prepared printed top-contact p-type TFT devices with optimized high-k dielectric exhibited good performance with the effective mobility up to 8.9 $cm^2/V \cdot s$, ON/OFF ratio ~10^6, small hysteresis (170 mV), and subthreshold swing (SS) as low as 92 mV/dec at low operating voltage (±1 V). With this doping ink, printed bottom-gate/top-contact p-type SWCNT-TFTs could be converted into the air-stable n-type SWCNT-TFTs with well-balanced and symmetric performance (comparable to their p-type counterparts) in a single step of solution process. The n-type SWCNT-TFTs exhibited air stability with negligible ON current degradation and V_{ON} shift for over 6 months long period. Matching n-type and p-type TFTs electrical characteristics enable to fabricate low-voltage CMOS inverters and NAND logic gates. The CMOS inverters can operate correctly at a supply voltage (V_{DD}) down to 0.3 V with a voltage gain as high as 22 at V_{DD} = 1.1 V, a trip voltage of ~$V_{DD}/2$ and a noise margin of 0.42 V (76.4 % of $V_{DD}/2$). More importantly, CMOS inverters show good air stability after 3 months with negligible static performance degradation. In addition, the NAND gates can work well without any voltage loss at input voltages of 1 V.

2. Experimental section

2.1. Materials and instruments

Arc discharge carbon nanotubes were purchased from Carbon Solutions (USA). PFIID (Isoindigo-based poly(9,9-dioctylfluorene) derivative, synthesized by ourselves[30]. Silver nanoparticles ink was obtained from Advanced Nano Products Co, DGP 45HTG. The epoxy amine ink used for n-doping and encapsulation was purchased from Xuzhou (China) Zhongyan Technology. The ink contains two compounds: the epoxy resin (128) and the cross-linking agent (ZY-F51). Optical absorption measurements were performed in a Perkin Elmer Lambda 750 UV-Vis-NIR spectrometer. All the electrical measurements of SWCNT-TFTs were carried out using a Keithley 4200 in air. The field effect mobility of SWCNT-TFTs were calculated with the standard linear regime relation $\mu = (\frac{\mathrm{d}I_D}{\mathrm{d}V_{GS}}) \times \frac{L}{W} \times \frac{1}{V_{DS}C_i}$[31]. The input signal was generated by Tektronix AFG 3052C dual channel arbitrary function generator. The dynamic responses of inverters and NAND were performed by Tektronix MSO 2024 mixed signal oscilloscope.

2.2. Preparation of sc-SWCNT inks and the epoxy amine inks

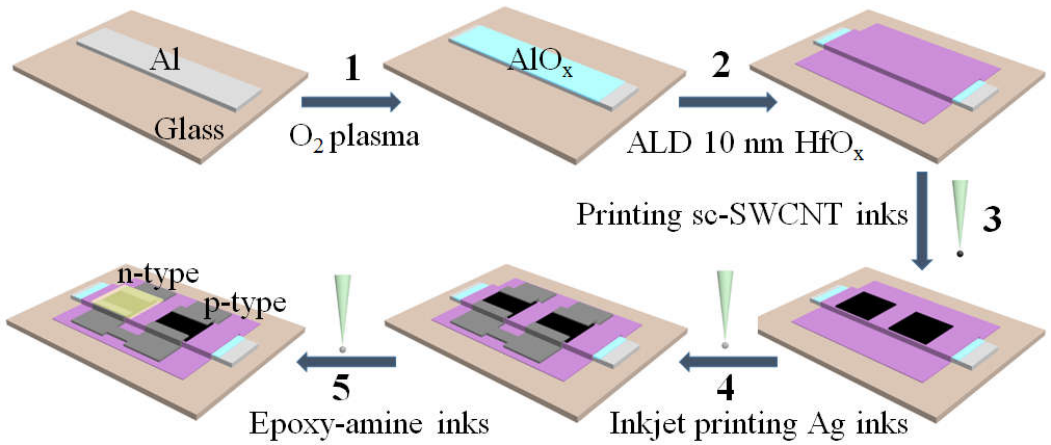
To obtain printable sc-SWCNT inks, 6 mg of arc discharge carbon nanotubes and 4 mg of PFIID were added into 10 mL toluene, and then homogenized for 30 min at 0 °C via probe-ultrasonication (Sonics & Materials Inc., Model: VCX 130, 60 W). Afterwards, the resulting SWCNT dispersions were centrifuged at 40 000 g for 2 h to remove the bundles and metallic species. The supernatants were drawn out from the

centrifuge tube and used to print SWCNT-TFTs without any other purification. The epoxy amine ink was formulated by mixing two chemical components (the epoxy resin (128) and the cross-linking agent (ZY-F51) with a weight ratio of 5:1). Then, the mixtures were stirred for half an hour at room temperature. As-prepared epoxy amine ink could be drop-casted onto the device channels without any other purification.

2.3. Fabrication and electrical properties of printed SWCNT-TFTs and logic circuit on glass substrates

The fabrication process of printed SWCNT-TFTs and CMOS inverters was illustrated in **Scheme 1.** Aluminum bottom gates (thickness of 30 nm) was firstly deposited onto the glass substrates by thermal evaporation through shadow mask to pattern the gate electrodes. Then, the samples were treated by O_2 plasma (5 min, 140 W) to form AlO_x layer over aluminum gates. For bilayer dielectric devices, 10 nm thick HfO_x thin films were deposited onto the plasma AlO_x layers via ALD (Cambridge NanoTech Inc.) at 250 °C. For the printed top-contact TFT devices, sc-SWCNT solutions were subsequently deposited in the device channels by aerosol jet printing (Optomec's M3D aerosol jet printing system) with a printing speed of 1.5 mm/s, and then washed with toluene 3 times. Finally, the devices were baked in air at 120 °C for 30 min for the removal of residual solvents. Silver nanoparticle inks (Advanced Nano Products Co, DGP 45HTG) were printed onto the SWCNT networks with a Dimatix Printer DMP-2831 to form source and drain electrodes and sintered on the hot plate at

150 °C for 30 min. The channel length (L) and width (W) were respectively 50 and 1000 μm. Conversely, SWCNT solutions were printed after the silver electrode printing for bottom-contact TFT devices. For TFT devices doped with the epoxy amine ink, the solution was selectively deposited onto device channels through a solid mask made of SEBS, followed by soft baking in an oven. Samples were heated up with a ramp rate of 2 °C min^{-1} from 60 to 120 °C and maintained at 120 °C for 5 min.



Scheme 1. Schematic illustration of the fabrication steps of printed SWCNT CMOS inverters on glass substrates.

3. Results and discussions

3.1. Printed p-type SWCNT-TFTs

Standalone electronic devices are likely to be powered by thin film batteries[32] or solar cells [33], requiring transistors to operate at a fraction of a few volts. To achieve low-voltage and high-performance SWCNT-TFTs and circuits[34,35], high capacitance dielectrics are commonly used and can be obtained with high dielectric constant (high-

k) materials and/or ultrathin layers. In this study, two kinds of dielectrics were therefore evaluated to develop p-type and n-type SWCNT-TFTs: mono-layer and bi-layer high-k dielectrics.

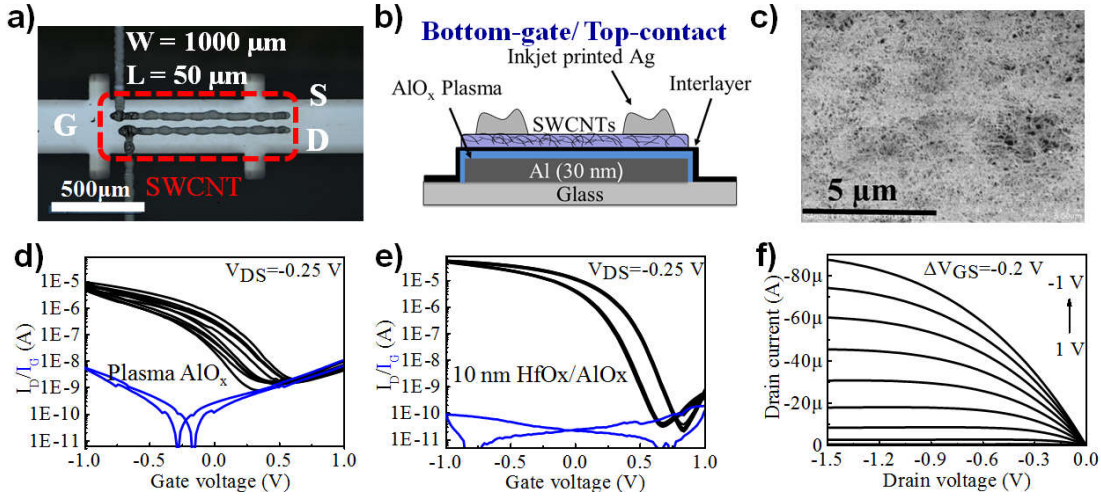


Figure 1. a) Optical image and b) schematic of a bottom-gate/top-contact printed SWCNT-TFT with channel dimensions: L= 50 µm and W = 1000 µm, c) SEM image of the printed SWCNT thin film in the device channel, d) several transfer curves of printed SWCNT-TFTs using plasma AlO_x thin films as dielectric layers at V_{DS}= -0.25 V, e) transfer curves and f) representative output characteristics of printed SWCNT-TFTs using 10 nm HfO_x/AlO_x thin films as dielectric layers.

Figure 1a and **1b** show the schematic of the device architecture and the optical image of a printed SWCNT-TFTs with the bottom-gate/top-contact configuration. The channel length and width of devices are 50 µm and 1000 µm, respectively. For printed SWCNT-TFT devices with one layer of dielectric, aluminum-evaporated gates were

simply exposed to oxygen plasma for 5 min (140 W), resulting in the formation of a ultrathin AlO_x layer (called "plasma AlO_x")[36]. For printed SWCNT-TFT devices with bilayer dielectric, 10 nm of HfO_x was deposited onto plasma AlO_x by ALD. Sc-SWCNT thin films were sequentially deposited by aerosol printing, followed by the deposition of silver source/drain electrodes by inkjet printing. Printable sc-SWCNT inks were sorted by isoindigo-based poly(9,9-dioctylfluorene) derivative (PFIID). The UV-Vis-NIR absorption spectrum of a sc-SWCNT ink is shown in **Figure S1a**. The semiconducting peaks in the range of 800-1200 nm are very sharp with a height about 0.37 to ensure the devices with high I_{ON}/I_{OFF} ratio. After printing sc-SWCNT inks, scanning electron microscopy measurements (SEM) were carried out to ensure the presence of SWCNT in the device channels (**Figure 1c**). From the SEM image, dense and homogeneous SWCNT networks could be observed in the TFT channels, regardless of the underlying dielectric. Performance of dielectric layers were assessed by measuring C-V curves of capacitors (metal/insulator/metal (MIM)) and the electrical properties of SWCNT-TFTs. For plasma AlO_x dielectric, electrical measurement performed on MIM structure (Al/plasma AlO_X/Ag) shows large areal capacitance of 1.78 μF/cm^2 at 1 Hz (**see SI Table 1**) with high leakage current density at 1 V (3 μA/cm^2, **Figure S1c**). The electrical behavior of transistor in linear regime is consistent with MIM measurements (transfer curves, **Figure 1d)** with high gate leakage current (5 nA at V_{GS} = -1 V), leading to low ON/OFF current ratio (10^3) and large subthreshold swing (SS) of 258 mV/dec **(see SI Table 1**). To resolve the gate leakage issues, 10 nm of high-

k HfO_x thin films were deposited on top of plasma AlO_x thin films by ALD. Transfer characteristics of printed SWCNT-TFTs are presented in **Figure 1e,** which show good uniformity. Printed SWCNT-TFT devices worked well at low gate voltage (±1 V) and showed SS of 92 mV/dec due to high areal capacitance (1.25 μF/cm^2 at 1 Hz, **Figure S1b**). Besides, ON/OFF current ratio of 10^6 and low leakage current 200 pA at gate voltage of -1 V were obtained, confirming that high quality HfO_x layers provided strong gate control and low leakage current density simultaneously (**Figure S1b** and **Figure S1c).** Finally, it is worthy to note that output characteristics **(Figure 1f)** showed a linear behavior at low drain voltages, which indicates good ohmic contacts between the printed silver source/drain and printed SWCNT thin films.

3.2. Printed n-type SWCNT-TFTs and their air stability

In the literature, polarity conversion from p to n-type TFTs is usually attributed to the doping of SWCNT both in the channel and at the contacts[20–23]. Thus we wanted to check whether the contact configuration had an effect on the n-type doping efficiency. For this purpose, an n-dopant ink was explored with both top/bottom-contact configurations fabricated on 10 nm HfO_x/AlO_x/Al glass substrates, as shown in **Figure 2a** and **2b**. We speculated that cross-linked n-doping layer would be advantageous for air-stable devices. Therefore, an epoxy crosslinkable ink formulated by mixing an epoxy resin (Bisphenol A type polymer) with a cross-linking agent containing n-doping amine group[20,25,26,37] was selected (see **Figure S2a and 2b**). To convert p-type devices to their n-type counterparts, the epoxy amine ink was simply drop-casted on top of the

p-type transistor channels, followed by soft baking in an oven. The electrical properties of the resulting TFTs were assessed before and after epoxy amine doping process. Typical transfer characteristics at V_{DS} = ±0.25 V were measured for both top/bottom-contact devices before and after epoxy amine doping process, shown in **Figure 2c** and **2d**, respectively. At the same time, transfer curves of p-type and n-type top-contact SWCNT-TFTs in linear regime were performed at lower V_{DS} (± 0.05 V and ± 0.1 V) (**Figure S3a** and **Figure S3b**).

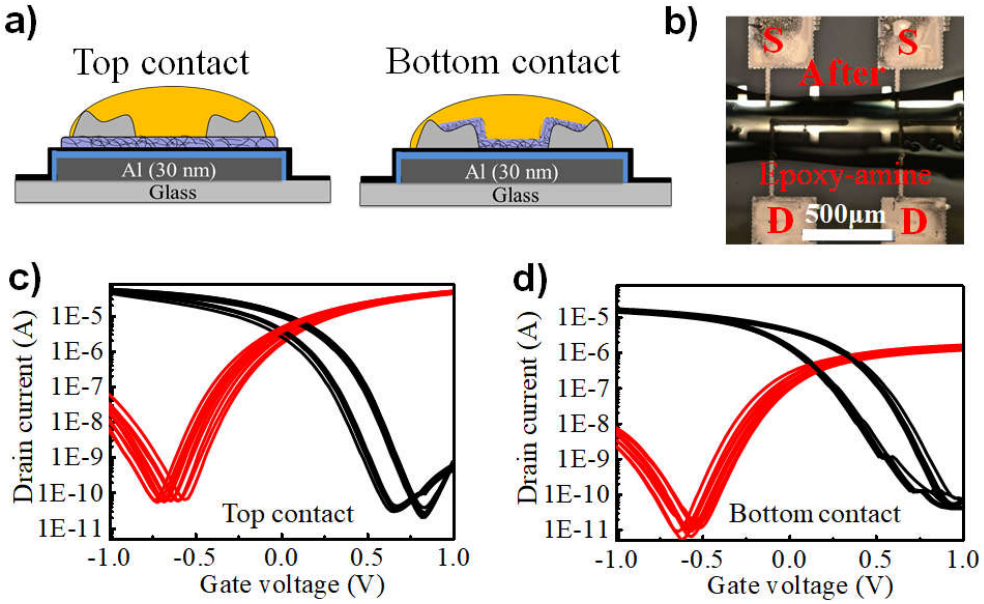


Figure 2. a) Schematic of printed bottom-gate/top and bottom contact n-type SWCNT-TFTs after drop-casting the epoxy amine ink onto the device channels and b) the corresponding optical image, transfer curves of printed c) bottom-gate/top-contact and d) bottom-gate/bottom-contact SWCNT-TFTs (Black curves (V_{DS}= -0.25 V) and red curves (V_{DS}= 0.25 V) represent printed p-type and n-type TFT devices, respectively).

Table1 Average electrical parameters and standard deviations (5 devices) extracted from the transfer characteristics in linear region at V_{DS} = -0.1 V and 0.1 V for p-type and n-type TFT devices, respectively.

	V_{TH} (mV)	V_{ON} (mV)	SS (mV/dec)	ΔV_{HYST} (mV)	I_{ON}/I_{OFF} ($\times 10^5$)	μ_{FE} ($cm^2/V \cdot s$)	$R_C \cdot W$[a] (kΩ)
TC-p-type	**228** ± 22	**670** ± 10	**92** ± 5	**170** ± 11	**20** ± 0.3	**8.9** ± 0.31	**2.5** ± 0.15
BC-p-type	**312** ± 14	**910** ± 10	**110** ± 7	**240** ± 10	**3** ± 0.4	**2.45** ± 0.08	**7.5** ± 0.4
BC-n-type	**-82** ± 49	**-600** ± 30	**120** ± 8	**45** ± 10	**2** ± 0.4	**0.33** ± 0.03	**82.5** ± 5
TC-n-type	**53** ± 37	**-660** ± 40	**87** ± 5	**20** ± 10	**6** ± 0.2	**9** ± 0.22	**1.2** ± 0.1

Notes: TC, BC, V_{ON}, SS, ΔV_{HYST}, I_{ON}/I_{OFF} and μ_{FE} represent the top-contact and bottom-contact configurations, the turn-on voltage, the subthreshold swing, the hysteresis extracted at V_{GS} from -1 to 1 V with a sweep rate of 0.25 mV/s, the ON/OFF current ratio and the linear field effect mobility, respectively - [a] The contact resistance (R_C) were calculated using the Y-function method.

Furthermore, the electrical properties of printed SWCNT-TFTs, such as the hole and electron mobility, current hysteresis, ON/OFF ratio and contact resistances were extracted and summarized in **Table 1**. Before drop-casting the epoxy amine ink, printed SWCNT-TFTs exhibit typical p-type behavior (**shown in Figure 2c** and **2d** black transfer curves). Comparison of p-type performance of the printed CNT-TFTs in top/bottom-contact configuration highlights differences in term of field-effect mobility and hysteresis. The printed bottom-contact SWCNT-TFTs demonstrate a larger hysteresis of 240 mV between the forward and reverse sweep, which is probably attributed to charge trapping[38] at the SWCNT/HfO_x interface along with absorbed water molecules in SWCNT films in the channel and at the contacts. In contrast, the top-contact TFT devices showed a smaller hysteresis of 170 mV because the SWCNTs were

partially encapsulated from water and oxygen by printed silver electrodes. For the field effect mobilities (μ_{FE}) extracted from the measured effective capacitance of printed SWCNT-TFT device at 1 Hz (as shown in **Figure S1b)**, top-contact TFTs show the effective mobility as high as 9 $cm^2/V \cdot s$, which is three times larger than those of the bottom-contact TFT devices.

The contact resistances, estimated using the Y-function method (**Table 1**), accounted very well for the differences between top-contact and bottom-contact saturated mobility. Top contacts provided a better coverage of the SWCNT and can prevent oxidation of printed silver electrodes (that injects charge into the channel) in air, which might explain their lower values of the contact resistances. After the polarity conversion with the epoxy amine ink, large differences between top-contact and bottom-contact SWCNT-TFTs could also be observed. For the top-contact devices, transfer curves of n-type devices were well-balanced and symmetric with the original p-type TFTs, while the bottom-contact devices exhibited an observable degradation of device performance after the polarity conversion. The on-state current of top-contact n-type TFT devices remained the same as those of p-type as well as the linear mobility. Besides, SS, hysteresis and contact resistance were improved after the deposition of epoxy amine inks on device channels, which could be attributed to the encapsulation from ambient moisture and oxygen. On the other hand, bottom-contact n-type TFTs showed significant degradation of device performance after the polarity conversion. The on-state currents of n-type TFT devices dropped from one order of magnitude

compared to the corresponding p-type devices, which is correlated to a 10 folds increase of the contact resistance (**Table 1**). The presence of the insulating epoxy at the interface between printed silver S/D electrodes and SWCNT thin films probably impeded the carrier injection from the contacts to the SWCNT networks, resulting in higher contact resistances. Significant contact resistances for n-type bottom-contact devices can also be observed from the output characteristics (**Figure S4a** and **Figure S4b**).

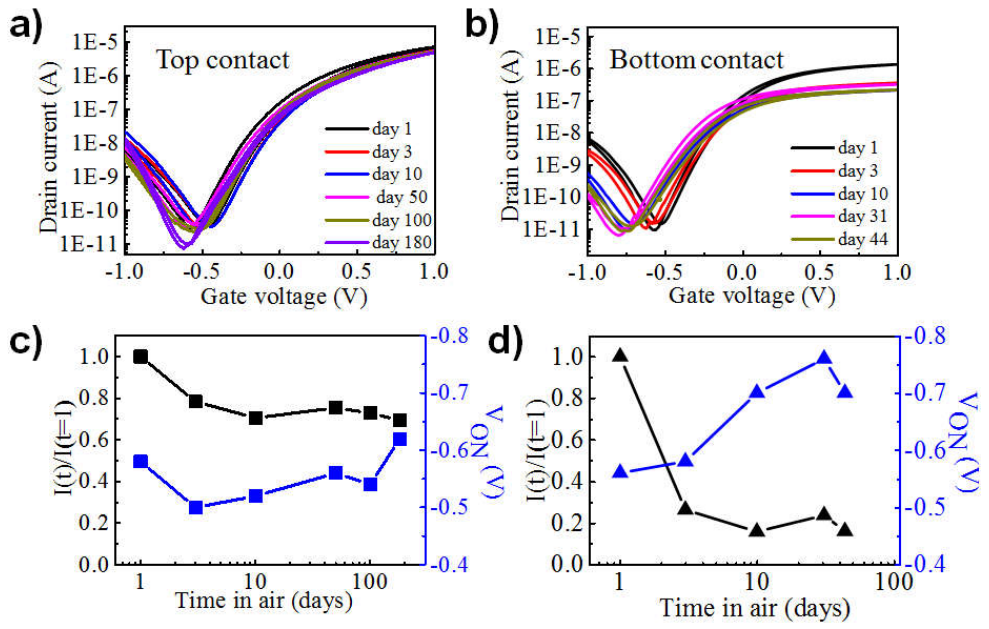


Figure 3. a) Evolution of transfer characteristics of the epoxy-amine doped and encapsulated top-contact n-type devices kept in air for 180 days and b) bottom-contact n-type devices kept in air for 44 days, and the variations of the normalized drain current degradation over time I_t/I_1 (t is the measuring day and t=1 corresponds to the day when the doping/encapsulation step was performed) and V_{ON} for c) the top-contact and d) bottom-contact TFT device.

In addition, the air stability of the SWCNT-TFTs after polarity conversion was

studied. Long-term air stability of the n-type SWCNT-TFTs is an essential requirement for the integration of TFTs in practical CMOS circuits. Diffusion of oxygen and water in the n-doped SWCNT layer is the main reason for the air instability of n-type devices, and the other one is the aging of doping material itself. In our case, the epoxy amine ink is a good candidate for air-stable n-type dopant as its cross-linked chemical structure would enable the device encapsulation. To confirm this assertion, transfer characteristics were measured for the top and bottom contacts from time to time during a period of 180 and 44 days respectively. As shown in **Figure 3a** and **3c**, the transfer curves of top-contact n-type devices only showed minor changes. After 180 days and without any recovery treatment, the ON current had a degradation of 31% while V_{ON} shift only from -0.5 to -0.62 V. The bottom-contact devices, on the other hand, exhibited poor air stability with I_{ON} degradation of 74% within 3 days, and a variation of V_{ON} from -0.56 to -0.7 V after 10 days (**Figure 3b** and **3d**). It is clear that top-contact geometry yields to better air stablility for n-type devices. To further demonstrate the potential of top-contact n-type SWCNT-TFTs for practical applications, the gate bias stress (negative and positive) measurements were performed in air for 2 hours. As shown in **Figure S5a** and **Figure S5b**, negligible threshold voltage shifts and On current degradations were observed after 2 hours, indicating an excellent operational stability of our n-type devices in ambient conditions.

3.3. Printed CMOS inverters and NAND gates

To demonstrate the potential of our polarity conversion method, printed CMOS

inverters and NAND gates were constructed by combining the p-type and n-type SWCNT-TFTs, as shown on **Figure 4a** and **Figure 5a**. The top-contact geometry was chosen due to their superior air stability and more balanced electrical characteristics of p/n-type transistors. **Figure 4b, 4c, 4d and 4e** present the static characteristics of CMOS inverters while important extracted static parameters have been gathered in **Table 2**. Rail-to-rail operation and trip voltages around $V_{DD}/2$ are the two criteria for CMOS logic circuits, since the output of one logic gate is the input for the next logic gate. In this study, all the measured inverters exhibited full rail-to-rail voltage operation at V_{DD} down to 0.3 V (**Figure 4b**). In addition, well-balanced and symetric electrical characteristics of the n-and p-type TFTs enabled trip voltages near the ideal values $V_{DD}/2$ (**Table 2**). On the other hand, the inverter gains shown in **Figure 4c** were from 22 to 1 at the input voltages of from 1.1 to 0.1 V, respectively, which is large enough to build more complicated circuits. Another impotant feature for portable devices is the power consumption. As shown in **Figure 4d**, the power consumption at the trip voltage of CMOS inverter were from 8.51 to 0.003 μW when the inverter was working at input voltage from 1.1 to 0.1 V (**Table 2**). The p/n-type TFTs in the inverter were already fully turned on for $V_{GS} > 0$ V with large ON current (>μA), which ultimately resulted in relatively high power consumption.

Table 2 The electrical parameters of printed CMOS inverters extracted from the static characteristics at different supply voltages (V_{DD})

V_{DD} (V)	0.2	0.3	0.4	0.5	0.6	0.75	0.9	1	1.1
V_{TRIP}[a] (V)	0.1	0.15	0.2	0.25	0.3	0.4	0.48	0.5	0.57
Gain[b]	2.5	4	6	7.5	10	12.5	15	17	22
P_W[c] (μW)	0.02	0.06	0.14	0.3	0.57	1.25	2.69	3.94	8.51

[a] the trip voltages of inverters, [b] the voltage gains of inverters at the trip voltage and [c] the power consumption at the trip voltage.

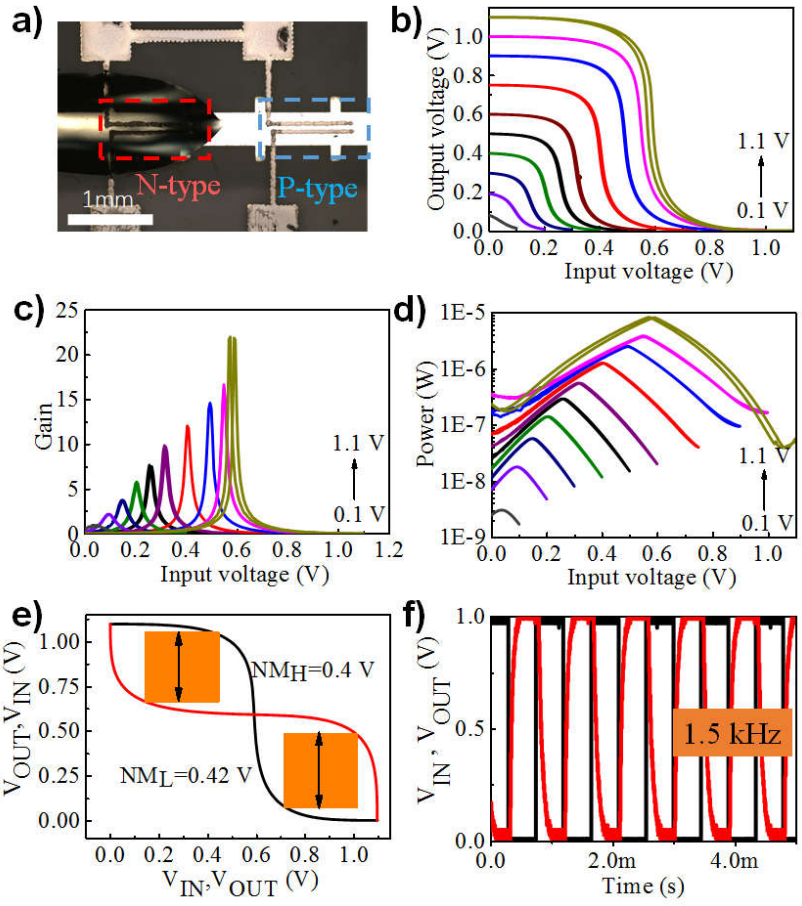


Figure 4. a) The optical image of a printed SWCNT CMOS inverter on the glass substrate, b) the voltage transfer curves, c) inverter gains, d) the power consumption of a printed CMOS inverter with the input voltages (V_{DD}) ranging from 0.1 to 1.1 V, e) the

noise margin of the printed CMOS inverter at input voltage of 1.1 V, f) the dynamic response of a printed CMOS inverter at 1.5 kHz (V_{DD} = 1 V).

The inverter noise margin (NM) for the CMOS inverter is also important since it is one of the key criterions of CMOS inverter design for enabling large-scale circuits. The noise margin of a typical printed CMOS inverter at the input voltage of 1.1 V is presented in **Figure 4e**. The noise margins for high state (NM_H) and low state ($NM_{L)}$ are 0.4 (NM_H 72.7% V_{DD}) and 0.42 V (NM_L 76.4% V_{DD}), respectively. Finally, the dynamic response of the inverter was investigated. (**Figure 4f**). For a 1.5 kHz input square-wave signal, the output signal showed a full rail-to-rail swing from ground to V_{DD}. Rising and falling times of the output signals were ~73 and ~85 μs, respectively, which confirms that performance of n-type and p-type SWCNT-TFTs were well matched. To compare the air stability and performance of our printed n-type devices and CMOS logic gates to other previous work, a summary of key metrics is given in **Table 3**. Among the reported chemical doping strategies without further encapsulations, our n-type TFT devices exhibit the longest period of air stability combined with the lowest ON current degradation. As a consequence, logic performance of the CMOS inverters could be also maintained for more than 3 months with a minimum trip voltage up-shift (0.05 V) due to the degraded performance of n-type TFT devices (**Figure S6a, b**). The excellent air stability for printed SWCNT CMOS inverters demonstrates the potential to develop the complex printed CMOS circuits.

Table 3 Comparison of the air stability of n-type SWCNT-TFTs based on chemical doping and performance of CMOS inverters

N-Dopant Materials	Stability[a] (t)	I_t/I_1 [b]	V_{DD} [c]	V_{TRIP}[d]	NM[e]	Gain[f]	P_W[g] (μW)	Ref.
Ethanolamine (EA)	30 days	35 %	-0.5 V	$2V_{DD}/3$, V_{DD}=-1 V	NM_H 103 % NM_L 40 % V_{DD}=-1 V	30, V_{DD}=-1 V	0.002	19
Epoxy based photoresist (SU8)	100 days	45 %	5 V	$5V_{DD}/8$, V_{DD}=20 V	None	15, V_{DD}=20 V	0.016	26
Viologen	80 days	46 %	None	None	None	None	None	22
NADH[h]	55 days	None	2 V	< 0V, V_{DD} = 2 V	None	<1, V_{DD} = 2 V	None	24
DMBI[i]	None	None	80 V	$V_{DD}/2$, V_{DD}=80 V	NM 70 %, V_{DD}=80 V	85, V_{DD}=80 V	None	20
Polyethyleneimine (PEI)	None	None	20 V	$2V_{DD}/5$, V_{DD}=20 V	NM_H 50 %, V_{DD}=20 V	7, V_{DD}=20 V	None	16
Epoxy amine	**180 days**	**69 %**	**0.3 V**	**$V_{DD}/2$, V_{DD}=1.1 V**	**NM_H 72.7 %, NM_L**	**22, V_{DD}=1.1 V**	**0.06**	**This work**

Notes: [a] Air stability in ambient conditions, [b] the normalized drain current degradation at t (I_t/I_1, "t=1" corresponds to the day when the doping/encapsulation step was performed), [c] the lowest driving voltage reported for the inverters, [d] the trip voltages of inverters, [e] the noise margins of inverters, [f] maximum voltage gains reported at V_{TRIP}, [g] Static power consumption at V_{TRIP} for the lowest reported V_{DD}, [h] β-Nicotinamide adenine dinucleotide, reduced dipotassium salt (NADH), [i] dimethyl-dihydro-benzoimidazoles.

A basic NAND gates were also fabricated on glass substrates (**Figure 5a** and **Figure 5b**). A NAND gate consists of two p-type TFTs in parallel and two n-type TFTs in series as shown **Figure 5c**. The output characteristics for the four possible input states of A and B of the NAND gates are shown in **Figure 5d**. In all cases, V_{in} (A and B) was set at V_{DD}=1 V for logic '1', and V_{in} was set at 0 V for logic '0'. Output voltages of '1' were observed when one or both inputs were applied '0'. Conversely, when both inputs were '1' , the output voltages were '0', confirming the proper logic operation of the

fabricated CMOS NAND gates. Moreover, ideal rail-to-rail output voltages swing without voltage loss was achieved as is the case for printed CMOS inverters.

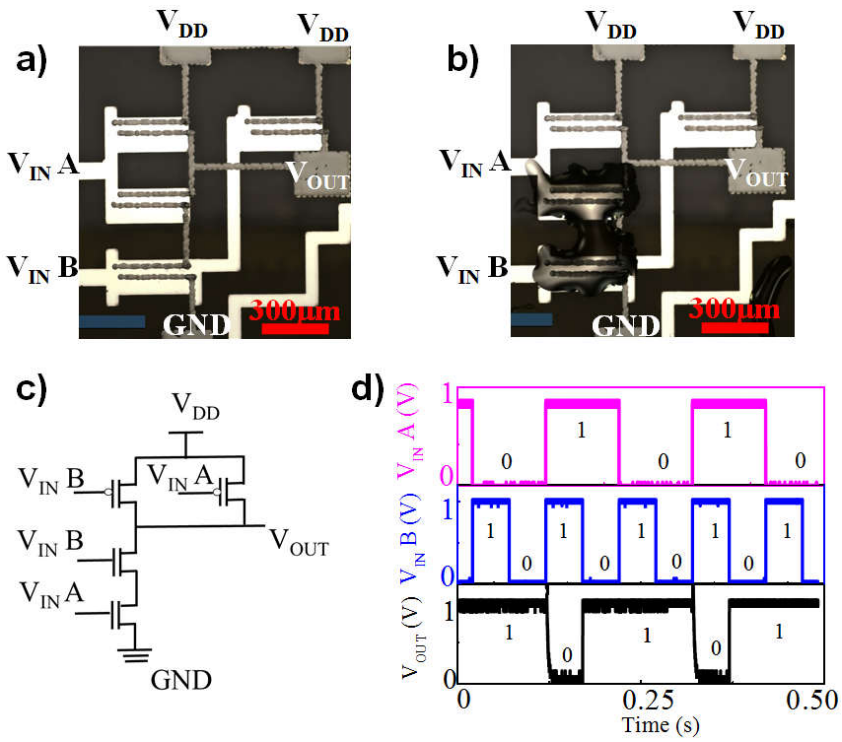


Figure 5. a) and b) the optical images of a printed NAND gate before and after drop casting the epoxy amine ink, c) a circuit diagram of a printed NAND gate, d) the output characteristics of the printed NAND gate. Input and output voltages of 0 and 1 V are regarded as logic '0' and '1', respectively.

4. Summary

We have developed an epoxy amine ink as an efficient n-dopant and encapsulant for sc-SWCNT thin films that enables the selective conversion from p-type to n-type transistor behavior. As-prepared printed p-type TFT devices using 10 nm HfO_x/AlO_x thin films as dielectric layers exhibited good performance with an effective mobility as

high as 8.9 cm²/V·s, high ON/OFF ratio (~10^6), small hysteresis (170 mV), and small SS (~92 mV/dec) at low operating voltage (±1 V). For optimized n-doping efficiency, both top-contact and bottom-contact configurations were compared in terms of the electrical properties and their air stability of printed n-type SWCNT-TFTs. The result demonstrated that top-contact TFT devices exhibited matched p/n-type performance and better air stability. As a demonstration of the realization of printed CMOS circuits, printed CMOS inverters and NAND logic gates were made using the top-contact p/n-type TFT devices. The printed CMOS inverters showed full rail-to-rail operation, trip voltages ~V_{DD}/2, voltage gain as high as 22, and noise margin of ~76.4% of V_{DD}/2 at V_{DD} = 1.1 V. In addition, printed CMOS inverters could operate correctly with V_{DD} down to 0.3 V with the power consumption of 0.06 μW, and remained stable in air as long as 3 months.

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Notes

The authors declare no competing financial interest.

Associated content

Supporting Information

Figures S1-S6 and Table S1 as described in the text:

Figure S1. Figure S1. a) Absorption spectrum of the PFIID-sorted sc-SWCNT ink, b) Areal capacitance of bare AlO_x (plasma-generated) and 10 nm HfO_x/AlO_x and c) the corresponding leakage current densities.

Figure S2. a) Cross-linked agent and b) bisphenol A epoxy resins.

Figure S3. Transfer curves of printed top-contact SWCNT-TFTs in linear regime. a) p-type at V_{DS}=- 0.05 and -0.1 V and b) n-type at V_{DS}=0.05 and 0.1 V.

Figure S4. Output curves of a) top-contact and b) bottom-contact n-type printed SWCNT-TFTs.

Figure S5. Gate bias stress measurements performed on the top-contact n-type SWCNT-TFTs in air for 7200 s with the conditions: a) negative bias stress (NBS) at polarization V_{DS}= 0.5 V and V_{GS}= -1 V and b) positive bias stress (PBS) at polarization V_{DS}= 0.5 and V_{GS} = 1 V. Note: Transfer characteristics were measured at V_{DS}= 0.25 V during the stress measurements.

Figure S6. a) The voltage transfer curves and b) voltage gains of a printed CMOS inverter after storage in air for 3 months.

Table S1 The areal capacitance at 1 Hz and leakage current at V_{GS}= -1 V of different dielectrics. The I_{ON}/I_{OFF} ratio and the subthreshold swing are the p-type SWCNT-TFT device performance with plasma AlO_x and 10 nm HfO_x/ AlO_x as dielectric layers.

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Miaomiao Wei and Malo Robin contributed equally to this work. This work was supported by Natural Science Foundation of China (61874132), the CAS President's International Fellowship for Postdoctoral Researchers (2019PT0020), National Key Research and Development Program of China (2016YFB0401100), Key Research Program of Frontier Science of Chinese Academy of Sciences (QYZDB-SSW-SLH031), and Basic Research Program of Suzhou Institute of Nanotech and Nano-

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Supporting information

Air-stable N-type Printed Carbon Nanotube Thin Film Transistors for CMOS Logic Circuits

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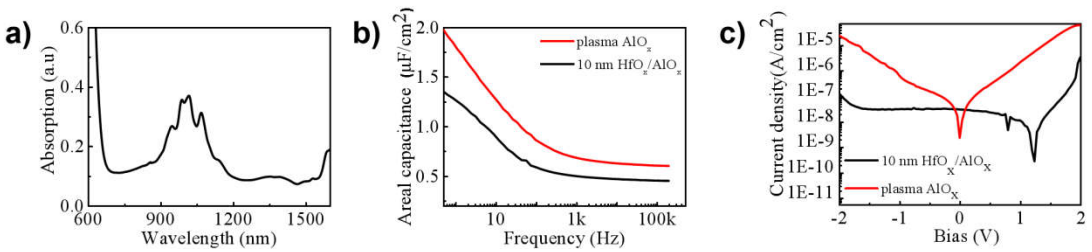

Figure S1. a) Absorption spectrum of the PFIID-sorted sc-SWCNT ink, b) the areal capacitance of bare AlO_x (plasma-generated) and 10 nm HfO_x/AlO_x thin films at V=-1 V and c) the corresponding leakage current densities.

Table S1 The areal capacitance at 1 Hz and leakage current at V_{GS}= -1 V of different dielectrics. The I_{ON}/I_{OFF} ratio and the subthreshold swing are the p-type SWCNT-TFT device performance with plasma AlO_x and 10 nm HfO_x/ AlO_x as dielectric layers.

Dielectric	Areal capacitance ($\mu F/cm^2$ at 1 Hz)	I_{ON}/I_{OFF} ratio	Leakage current (V_{GS} = -1 V)	SS (mV/dec)
Plasma AlO_x	1.78	10^3	5.61×10^{-9} A	258
10 nm HfO_x/ AlO_x	1.25	10^6	2.03×10^{-10} A	92

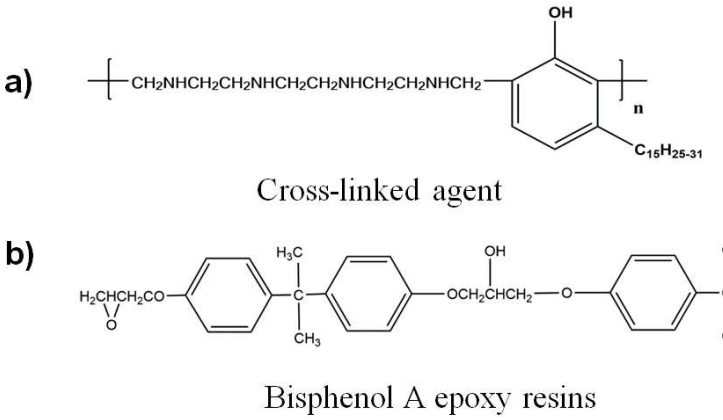

Figure S2. a) Cross-linked agent and b) bisphenol A epoxy resins.

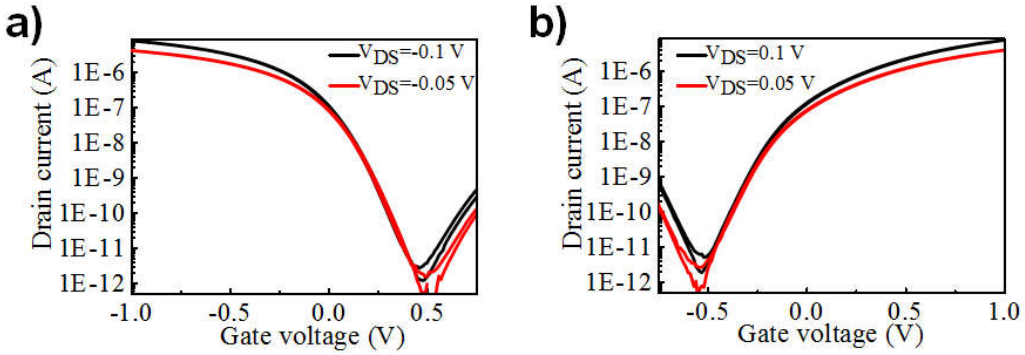

Figure S3. Transfer curves of printed top-contact SWCNT-TFTs in linear regime. a) p-type at V_{DS}= -0.05 and -0.1 V and b) n-type at V_{DS}= 0.05 and 0.1 V.

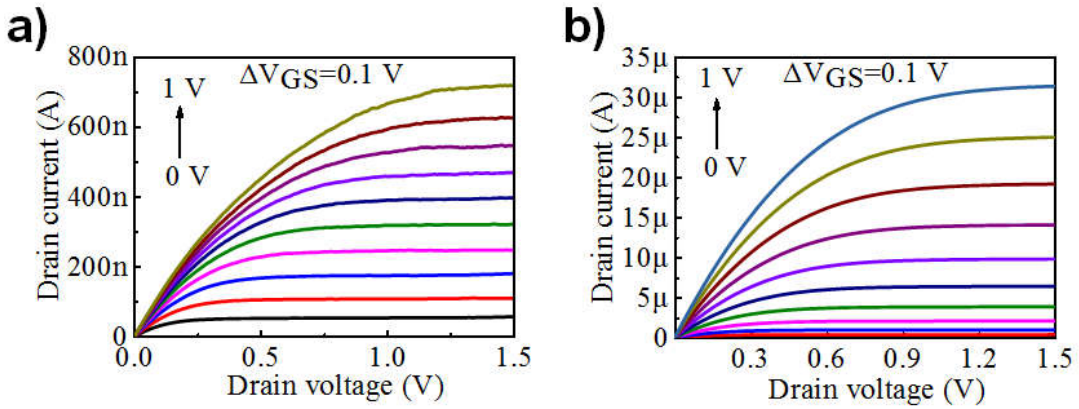

Figure S4. Output curves of printed a) bottom-contact and b) top-contact n-type SWCNT-TFTs.

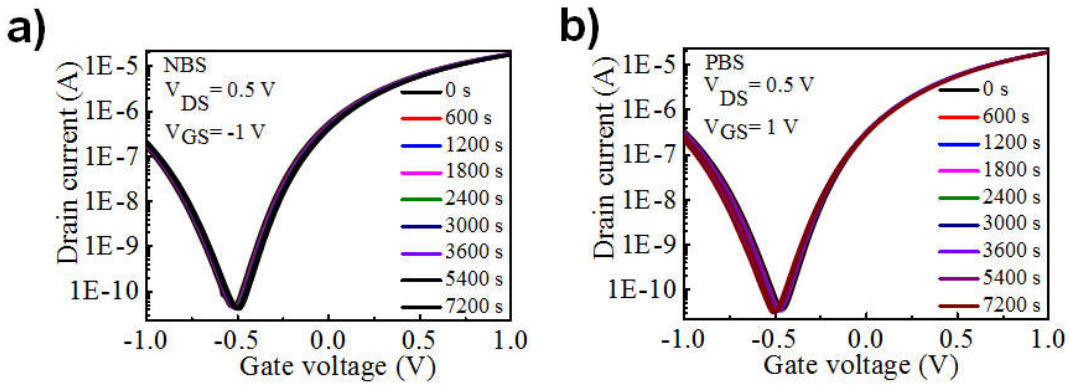

Figure S5. Gate bias stress measurements performed on the top-contact n-type SWCNT-TFTs in air for 7200 s with the conditions: a) negative bias stress (NBS) at polarization V_{DS}= 0.5 V and V_{GS}= -1 V and b) positive bias stress (PBS) at polarization V_{DS}= 0.5 and V_{GS} = 1 V. Note: Transfer characteristics were measured at V_{DS}= 0.25 V during the stress measurements.

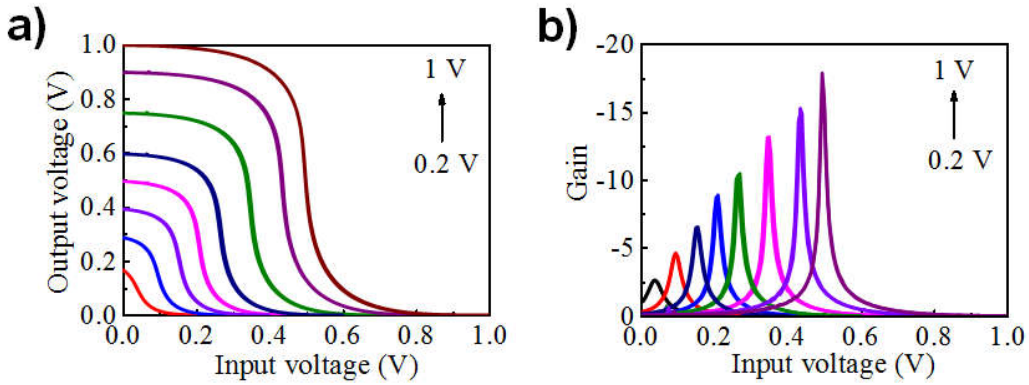

Figure S6. a) The voltage transfer curves and b) voltage gains of a printed CMOS inverter after storage in air for 3 months.

Credit author statement

Zhao Jianwen proposed and supervised the project. Zhao Jianwen, Cui Zheng, Pecunia Vincenzo and Cao Yu designed the experiment. Wei Miaomiao and Robin Malo prepared and measured p and n-type TFTs, and CMOS logic circuits; Portilla Luis prepared Al electrodes on glass and designed the NAND gates; Ren Yunfei characterized the SWCNT thin films by SEM; Shao Shuangshuang measured the dynamic responses of CMOS inverters; Bai Lan prepared sc-SWCNT inks and measured the absorption spectra of sc-SWCNT inks; Wei Miaomiao, Robin Malo, Cui Zheng and Zhao Jianwen analysed the data and co-wrote the manuscript. All the authors discussed the results and commented on the manuscript.